

Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
DDR III DIMM 1 / 2,DDR III DIMM 3 / 4	7,8
CLK GEN4106	9
CP-PCI/E/DMI/USB/CLK	10
CP-SATA/HOST/FAN/GPIO/VGA	11
CP-SMB/LPC/AUDIO/RTC/RST	12
CP-POWER,GND/NVRAM / Strap	13,14,15
ASM1083 PCIE to PCI Bri. / PCI Slot	16,17
PCIE Slot X16 / X1 / X8 / Pericom Switch	18,19,20
SIO-Fintek F71889AD/KB	21
1394 Controller - VT6315N-CE	22
LAN-RTL8111E	23
UPD720200F1 USB3.0 / USB3.0 PWR	24,25
UPD720200F1 USB3.0 / USB3.0 PWR	26,27
USB Connector	29
Audio Codec ALC892	31
ATX F_Panel/EMI/TPM	32
ACPI Controller UPI	33
SATA / FAN Control	34
VRD12 - uP6234 - 6Phase Dr.MOS	35,36
CPU_VTT - uP6103-1	37
CPU_SA - uP6103-1	38
DDR Power - uP6103-1Phase	39
PCH Power - uP6103-1Phase	40
PHASE Dropping & PSI & LED	41
XDP / Manual Parts	42

MS-7673

ATX(Full Size)
Ver: 20

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

ASM1083 PCIE to PCI Bri.
HD Audio Codec:RTL892
LAN:RTL 8111E 10/100/1000 NIC X 2
SIO:FIN71889AD(LAA)
FRONT USB3.0: UPD720200F1
REAR USB3.0: UPD720200F1
Flash ROM: 64 Mb SPI (PCH)
1394 Controller: VT6315N

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 2
PCI Express (X1) Slot * 4
PCI Slot * 2(From ASM1083)

PWM:

CPU:UPI6234(5PHASE)
CPU_VTT:UP6103A(1PHASE)
CPU_SA:UP6103A (1PHASE)
DDR/PCH PWR:UP6103A

ACPI:

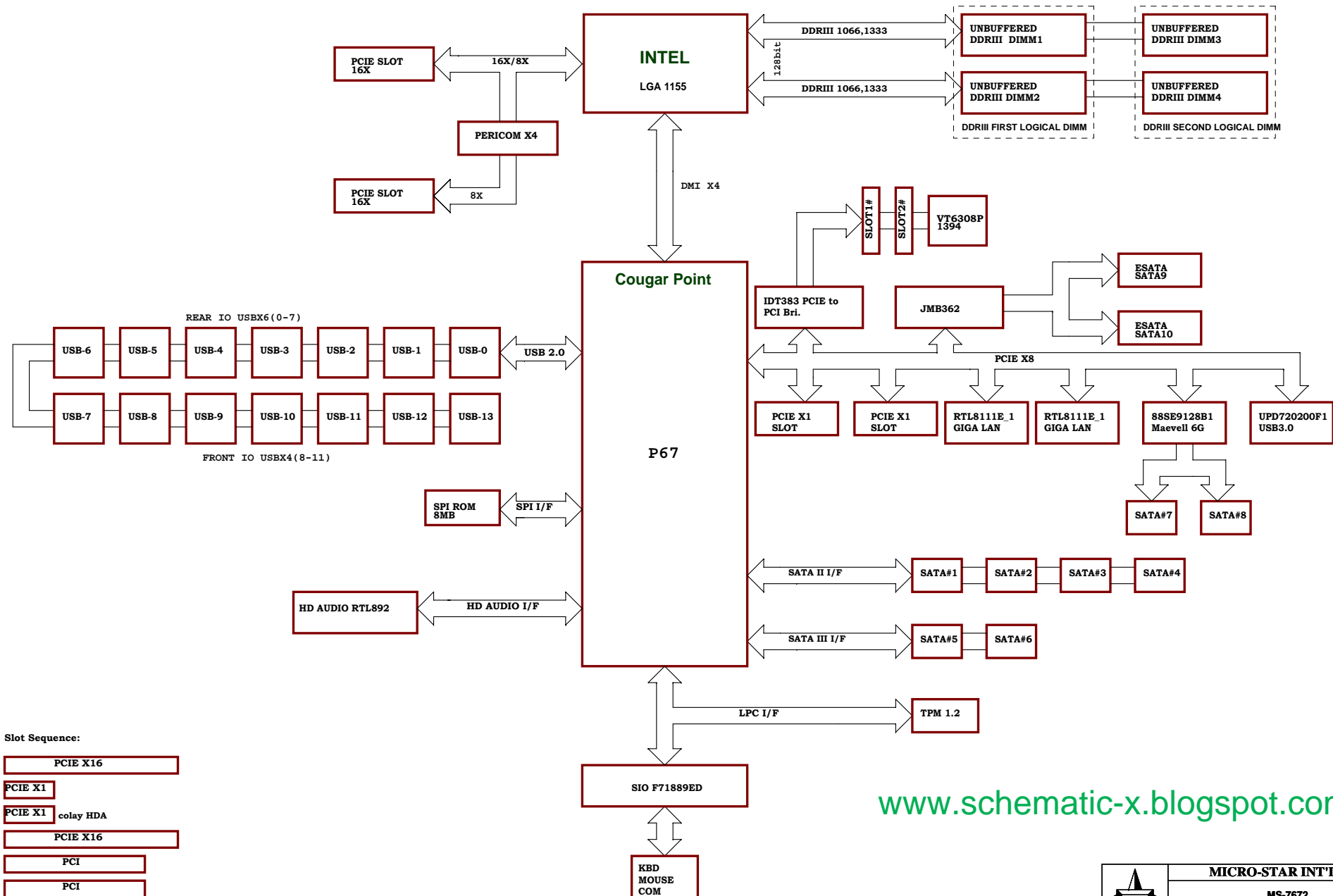
UPI

Other:

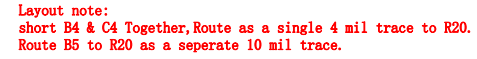
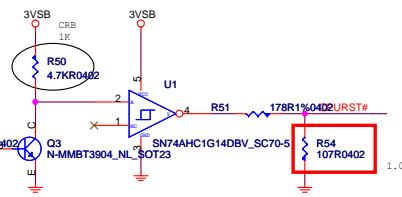
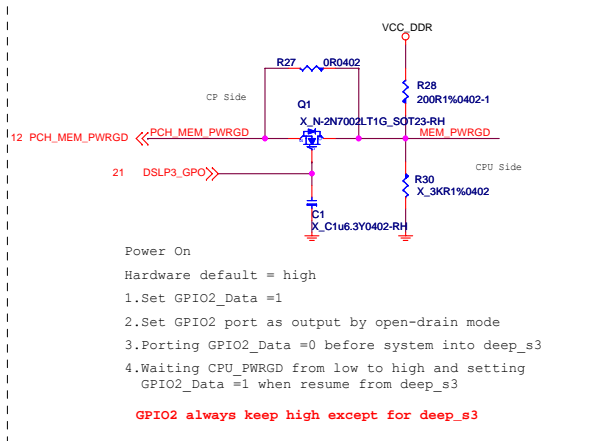
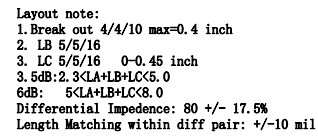
SATA3.0 x2+SATA2.0 x4 (PCH)
USB3.0 x4 (Rear*2 Front*2)
USB2.0 *4 (Rear*8 Front*4)
COM Header *1



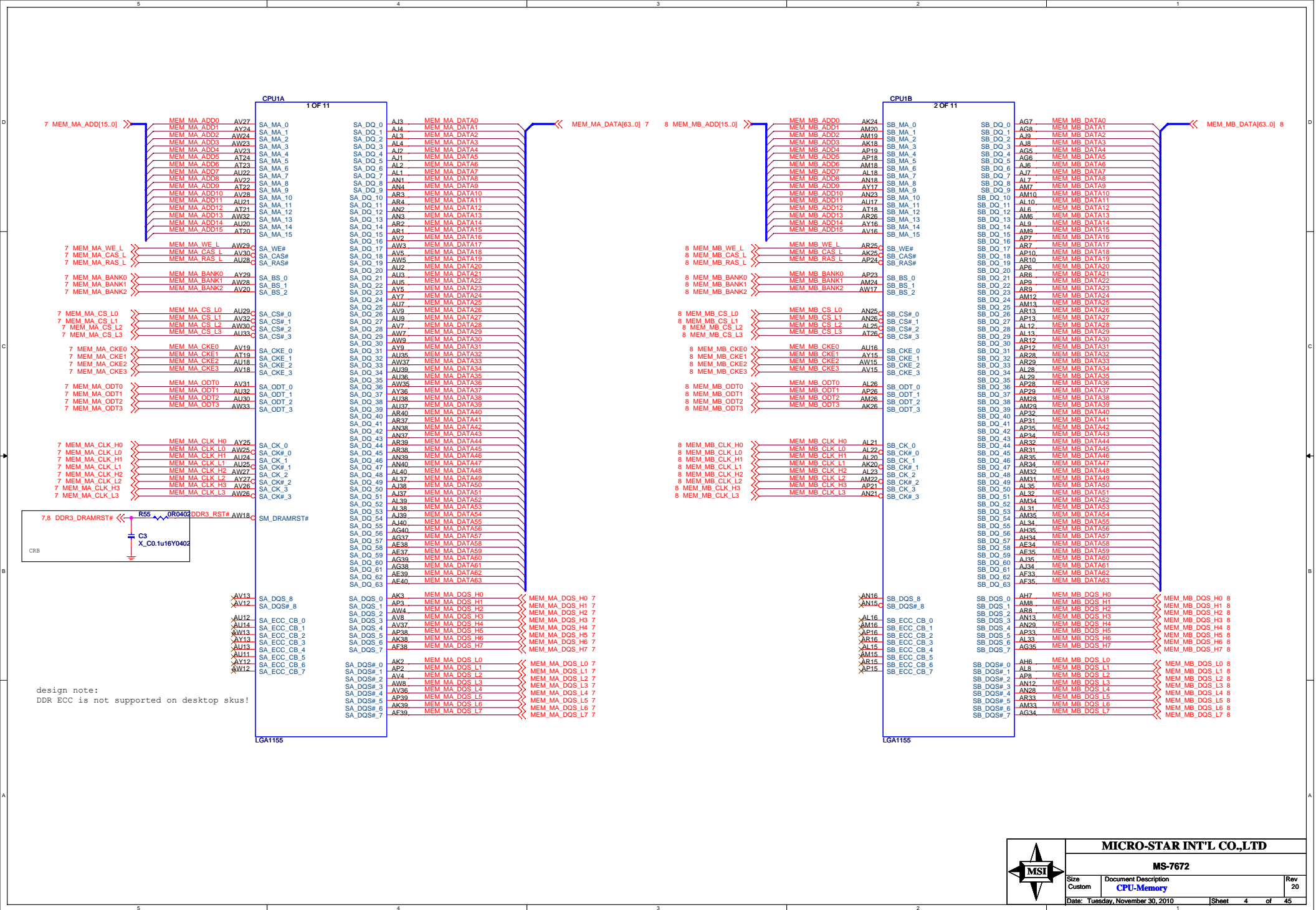
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MS-7673		
Size Custom	Document Description Cover Sheet	Rev 20
Date: Tuesday, November 30, 2010 Sheet 1 of 45		



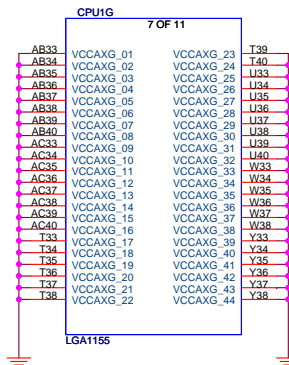
www.schematic-x.blogspot.com



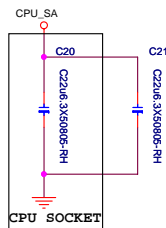
MICRO-STAR INT'L CO.,LTD			
MS-7672			
Size Custom	Document Description CPU-CNTL/CLK/MISC		Rev 20
Date: Tuesday, November 30, 2010		Sheet 3 of	45



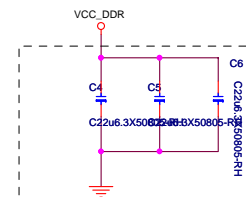
(1.05V / 1.00V)



```
VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 25A
VCC1_8: 1.6A
```

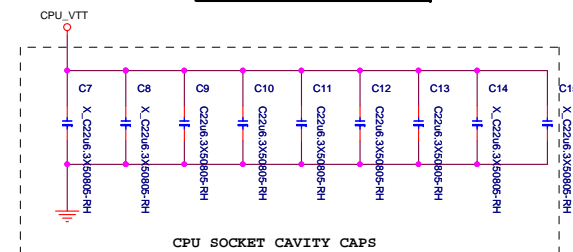


+1.5V_DDR3-Decoupling

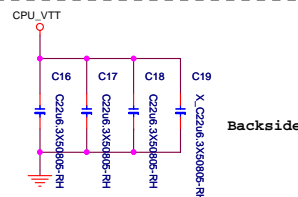


CPU SOCKET CAVITY CAPS

+CPU_VTT Decoupling

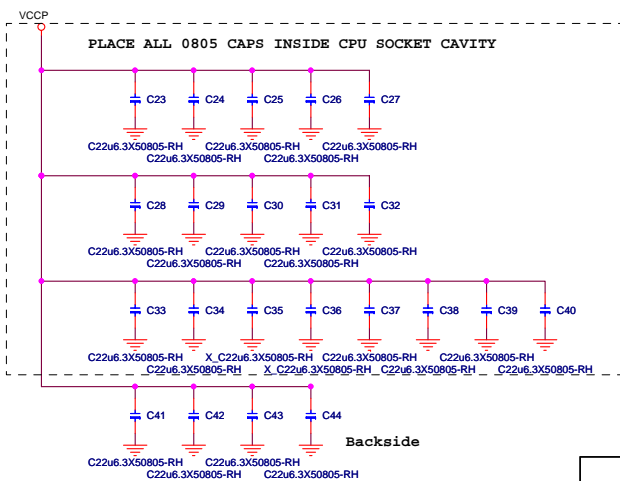


CPU SOCKET CAVITY CAPS



Backside

+CPU_VCCP-Decoupling



Backside



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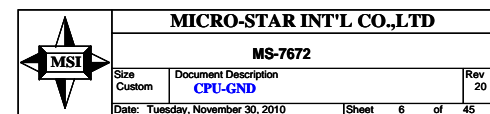
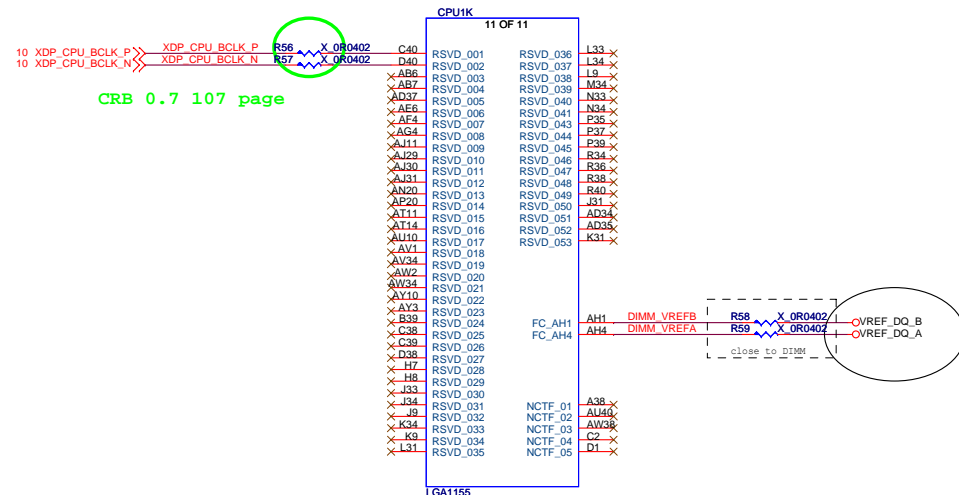
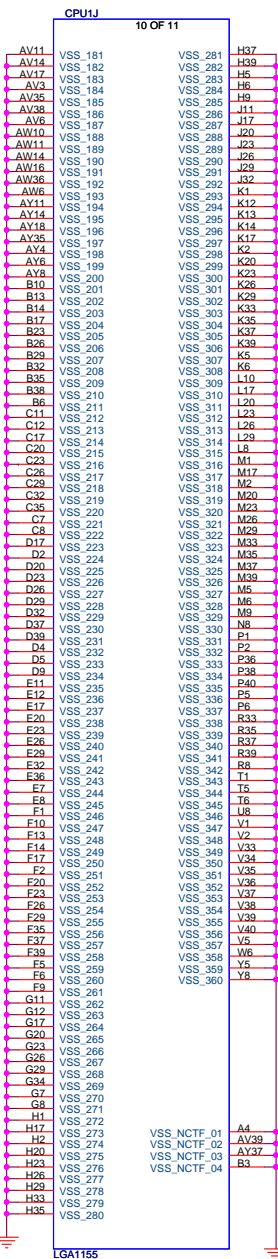
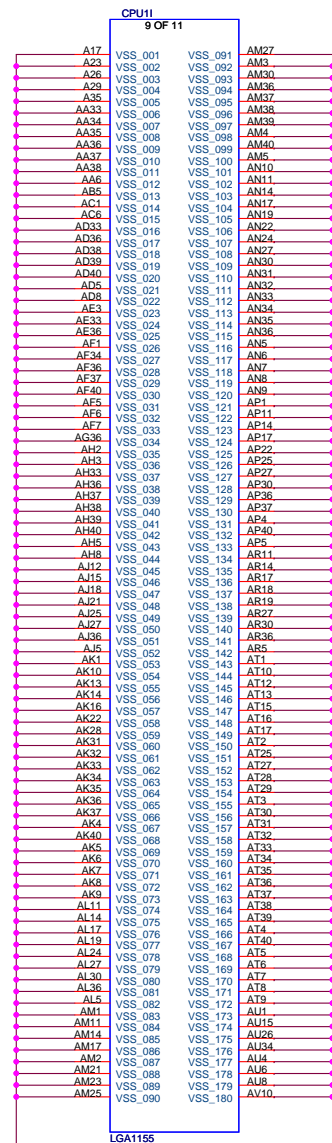
MS-7672

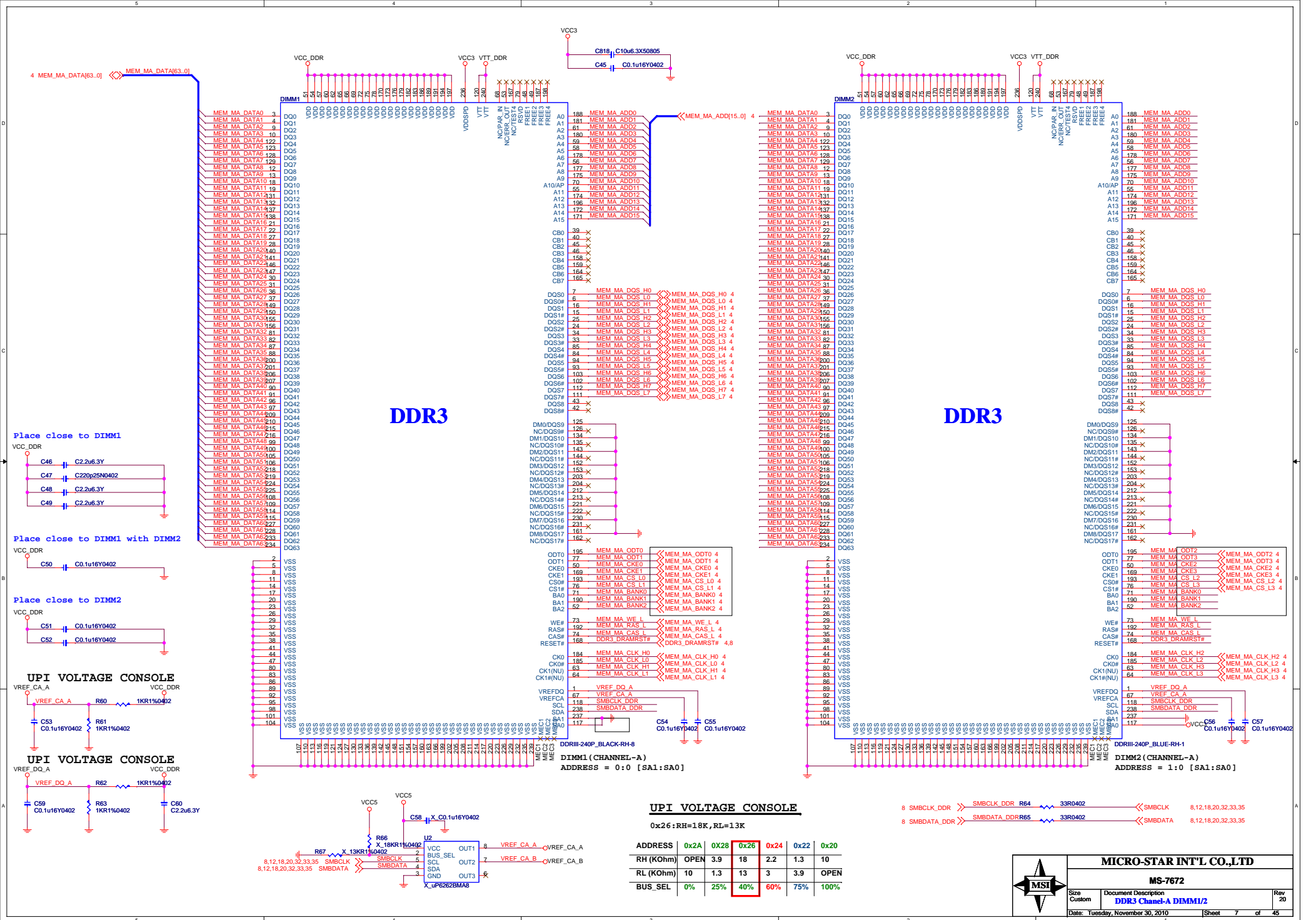
Size	Custom
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Document Description
CPU-Power

Date: Tuesday, November 30, 2010

Sheet 5 of 45





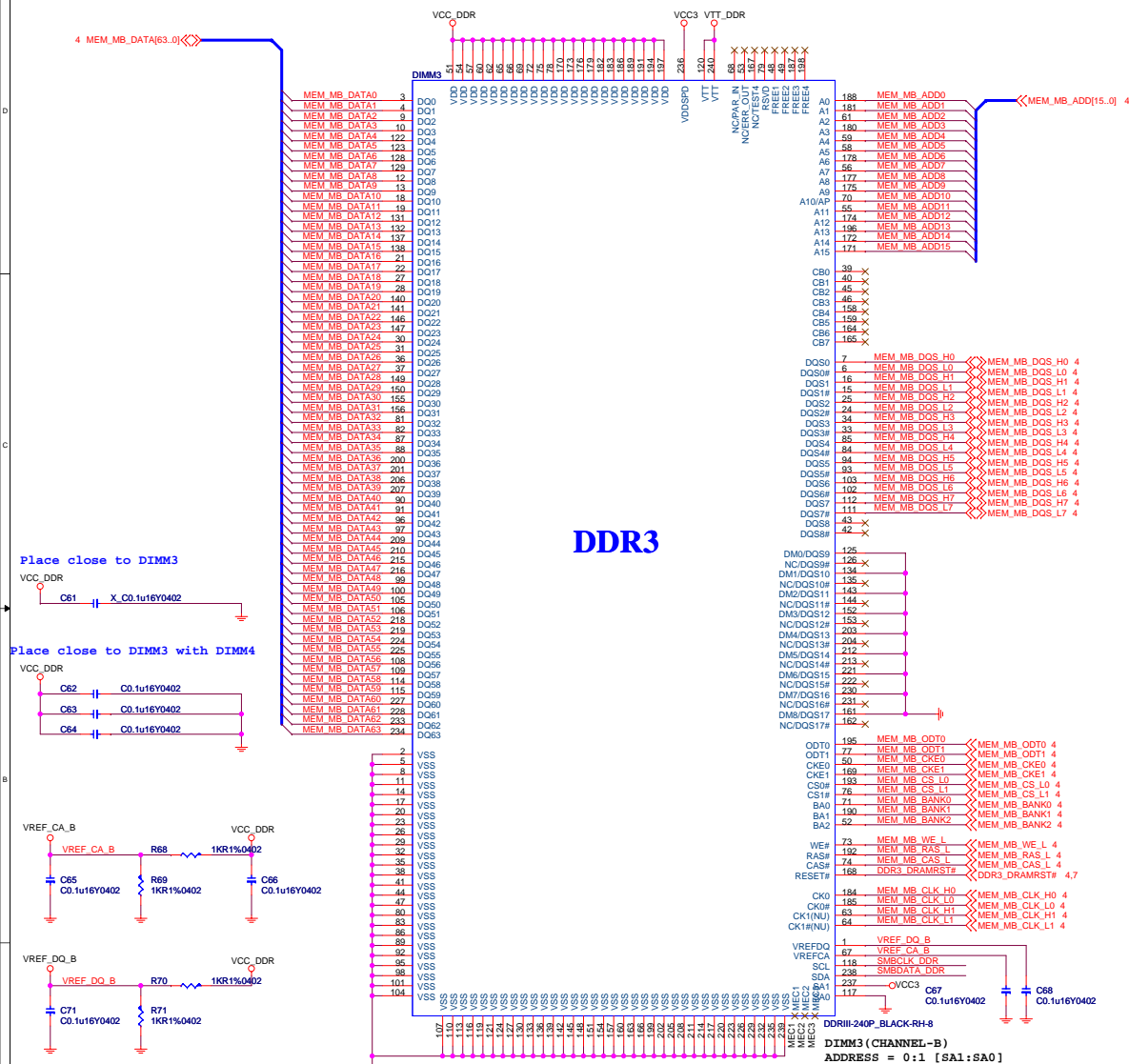
MICRO-STAR INT'L CO.,LTD

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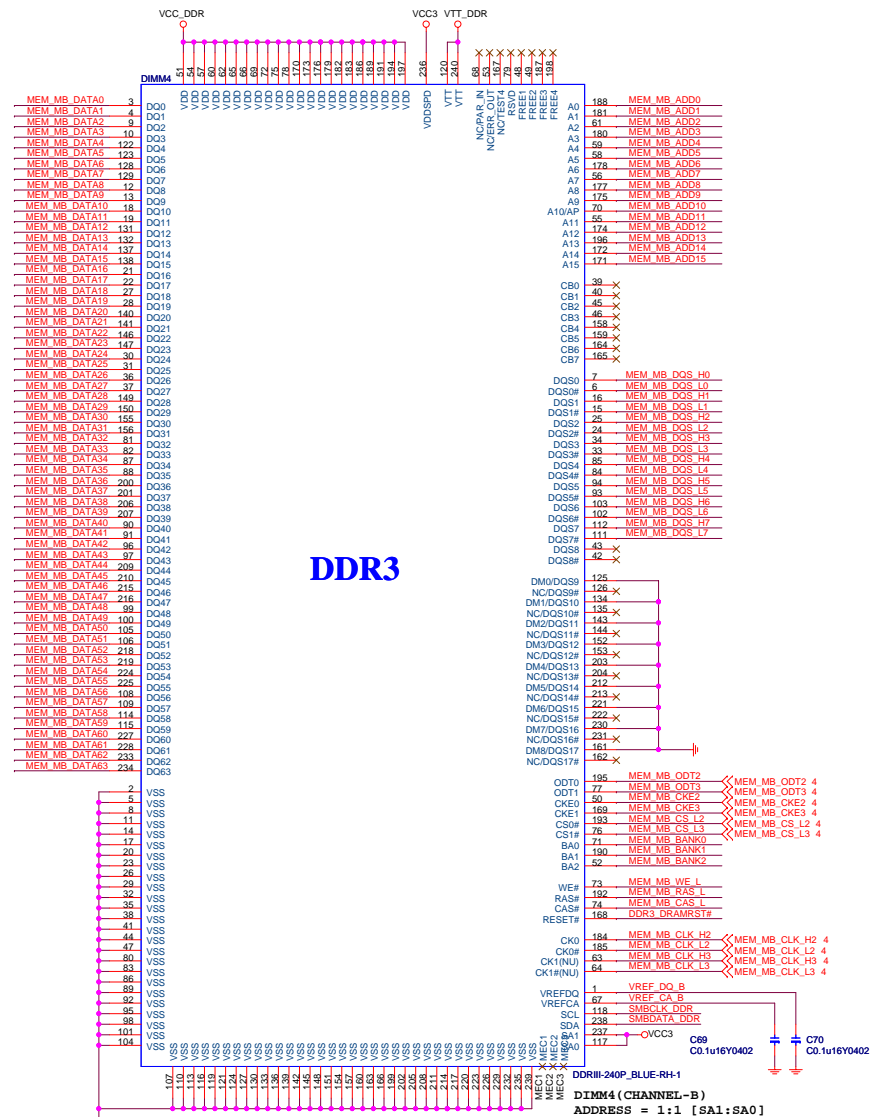
Document Description

Custom	DDR3 Chanel-A DIMM1/2	20
Date: Tuesday, November 30, 2010		Sheet 7 of 45

DDRIII DIMM_B0



DDRIII DIMM_B1



UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K

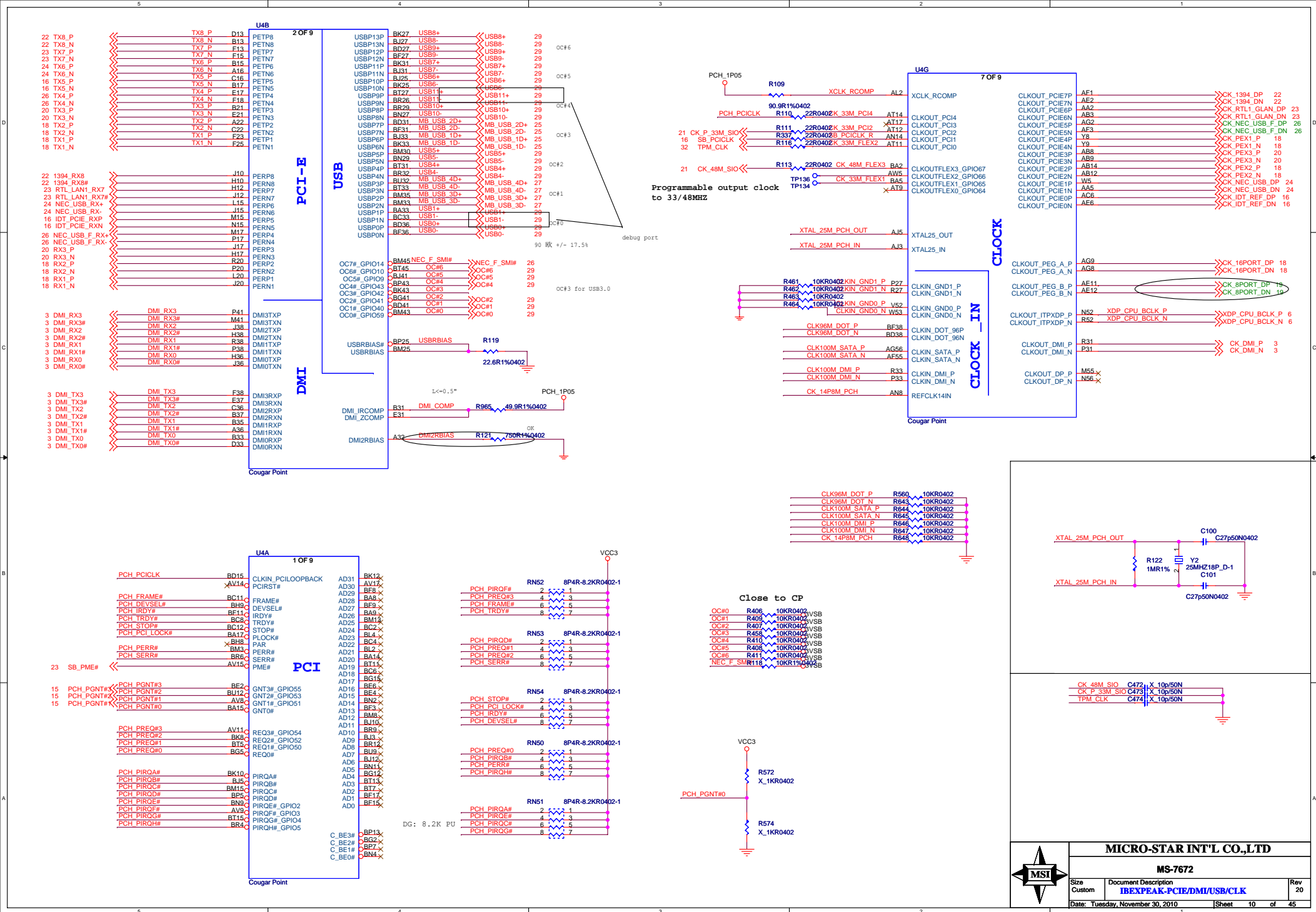
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	9.1	3	2.2	1.3	10
RL (KOhm)	10	3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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MS-7672

Size Custom	Document Description DDR3 Chanel-B DIMM3/4	Rev 20
Date: Tuesday, November 30, 2010		Sheet 8 of 45



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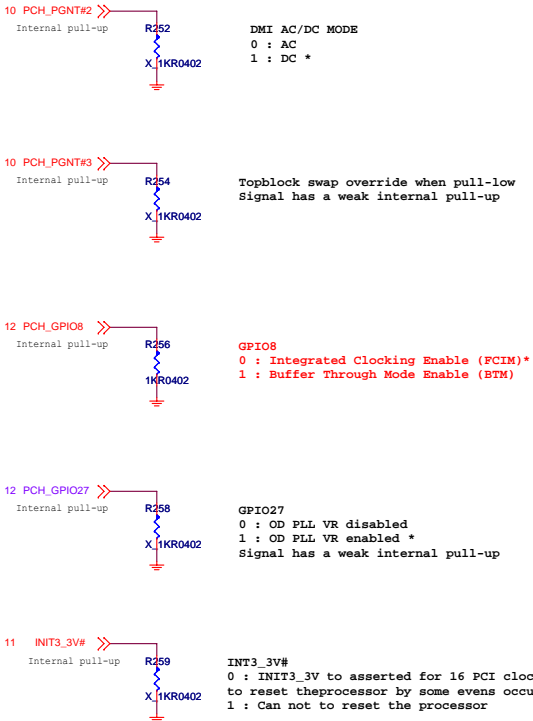
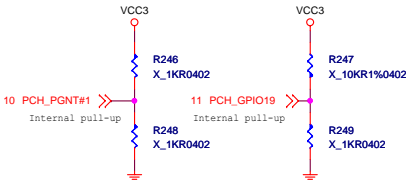
MS-7672

Size Custom	Document Description IBEXPEAK-PCIe/DMI/USB/CLK
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Date: Tuesday, November 30, 2010 Sheet 10 of 45

PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



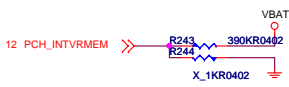
DMI AC/DC MODE
0 : AC
1 : DC *

Topblock swap override when pull-low
Signal has a weak internal pull-up

GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

GPIO27
0 : OD FLL VR disabled
1 : OD FLL VR enabled *
Signal has a weak internal pull-up

INIT3_3V#
0 : INIT3_3V to asserted for 16 PCI clock
to reset the processor by some evens occur
1 : Can not to reset the processor



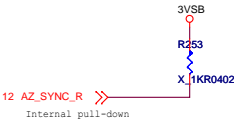
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the
integrated GbE only operates at 10/100 Mbps during S3-S5.



DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.
This signal enables the internal Deep Sleep 1.05 V
regulators. Must be connected even when not supporting DSW.

Internal pull-down

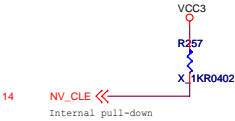


HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

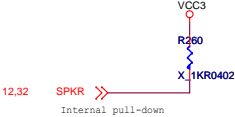
HDA_SYNC
OD FLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



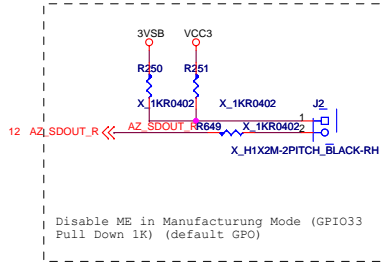
GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



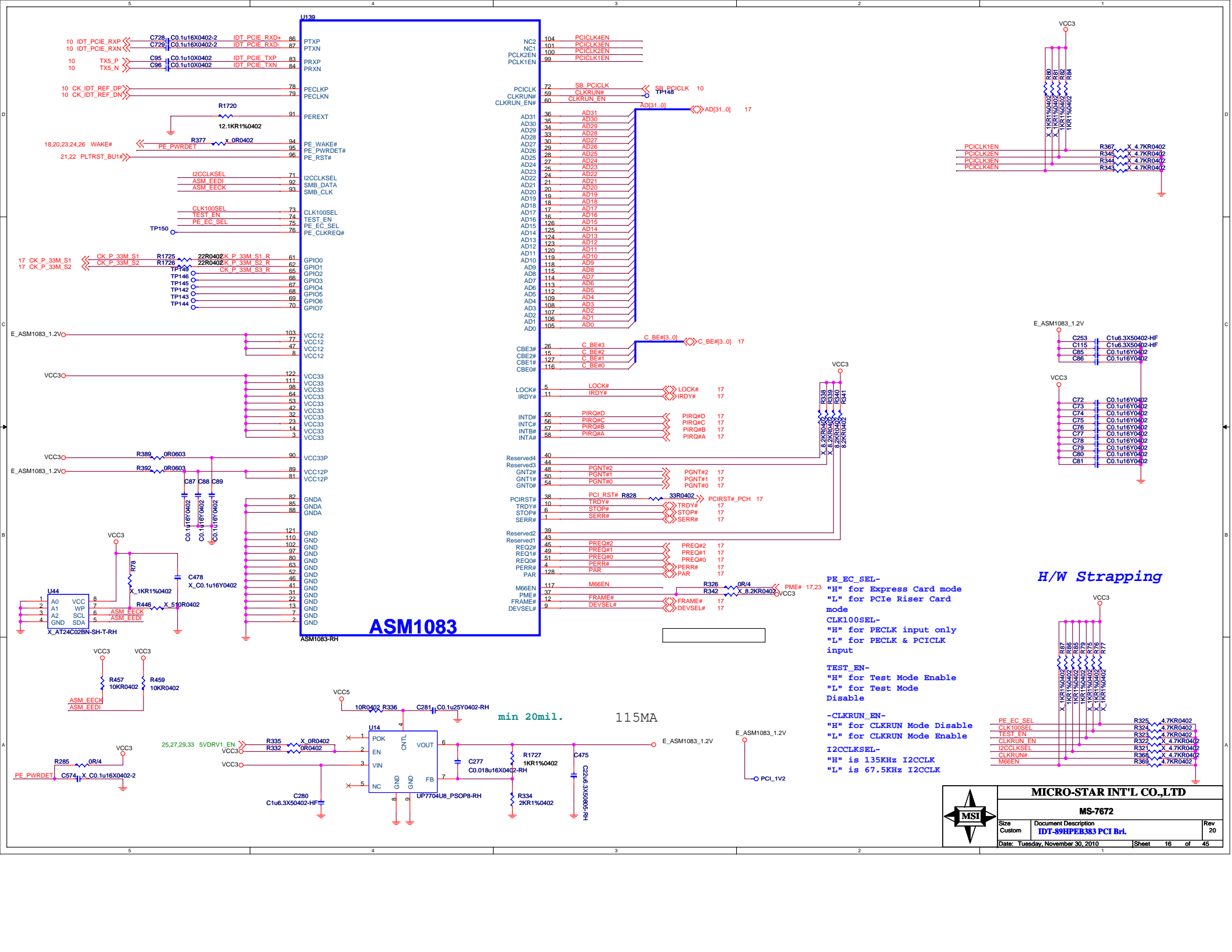
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

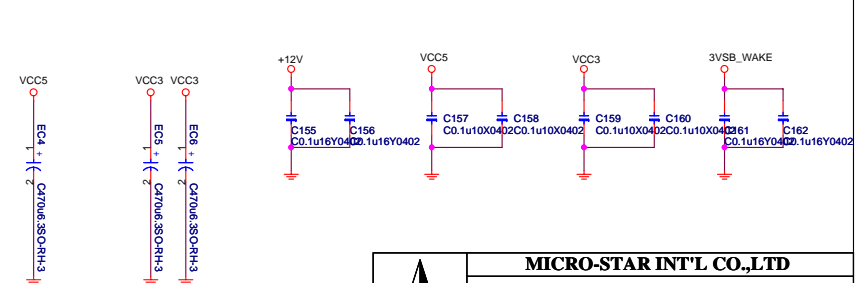
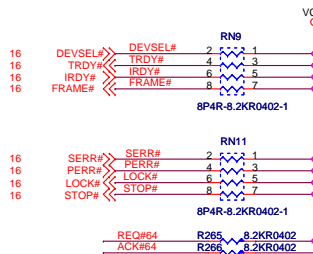
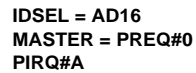


SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



MICRO-STAR INT'L CO.,LTD		
MS-7672		
Size Custom	Document Description Cougar Point-Strap	Rev 20
Date: Tuesday, November 30, 2010		
Sheet 15 of 45		

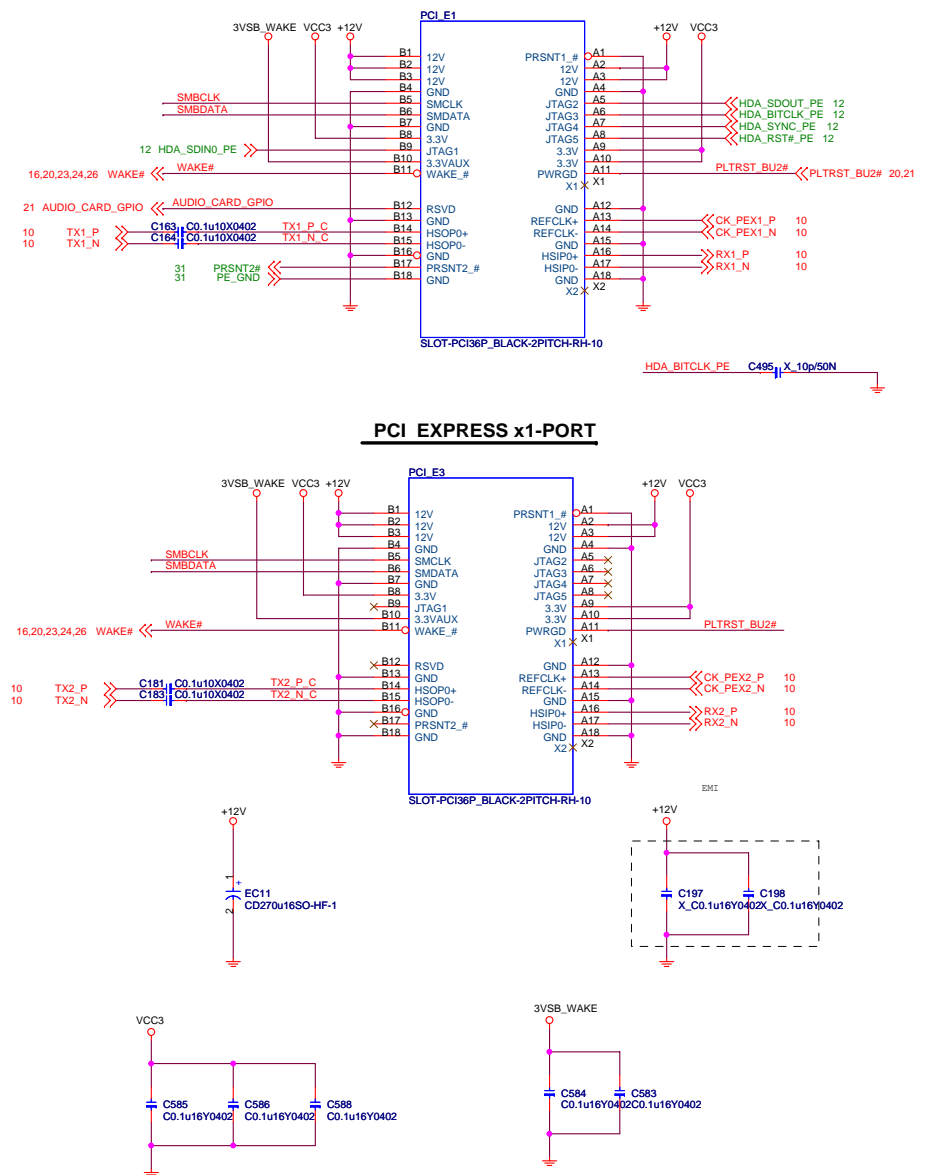




Size Custom	Document Description PCI Slot 1 & 2 & 3	Rev 20
Date: Tuesday, November 30, 2010	Sheet 17 of 45	

HDA co-lay PCIEx1

PCI EXPRESS x1-PORT



MS-7672

Document Description	PCIE x16, x1
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Friday, November 30, 2012

Rev
20

45

PCI Express X8 Slot (Share with PCI_E x16 Slots)

Switch AVL: I98-014300C-AD0

Trace width > 200 mils

7,8,12,18,20,31,32,34,41
7,8,12,18,20,31,32,34,41
3VSB_WAKE
16,18,20,23,24,26,43 WAKE#

PE_A_TXP8_S C202 C0.1u16X0402-2 PE_A_TXP8_SC
PE_A_TXN8_S C203 C0.1u16X0402-2 PE_A_TXN8_SC

PE_A_TXP9_S C204 C0.1u16X0402-2 PE_A_TXP9_SC
PE_A_TXN9_S C206 C0.1u16X0402-2 PE_A_TXN9_SC

PE_A_TXP10_S C207 C0.1u16X0402-2 PE_A_TXP10_SC
PE_A_TXN10_S C208 C0.1u16X0402-2 PE_A_TXN10_SC

PE_A_TXP11_S C209 C0.1u16X0402-2 PE_A_TXP11_SC
PE_A_TXN11_S C210 C0.1u16X0402-2 PE_A_TXN11_SC

PE_A_TXP12_S C214 C0.1u16X0402-2 PE_A_TXP12_SC
PE_A_TXN12_S C216 C0.1u16X0402-2 PE_A_TXN12_SC

PE_A_TXP13_S C216 C0.1u16X0402-2 PE_A_TXP13_SC
PE_A_TXN13_S C217 C0.1u16X0402-2 PE_A_TXN13_SC

PE_A_TXP14_S C217 C0.1u16X0402-2 PE_A_TXP14_SC
PE_A_TXN14_S C218 C0.1u16X0402-2 PE_A_TXN14_SC

PE_A_TXP15_S C219 C0.1u16X0402-2 PE_A_TXP15_SC
PE_A_TXN15_S C220 C0.1u16X0402-2 PE_A_TXN15_SC

within 500mil

3 DualX8_Enable << DualX8_Enable

SLOT-PCI164P_BLUE-2PITCH-RH-5

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

PE_A_RXP13_S

PE_A_RXN13_S

PE_A_RXP14_S

PE_A_RXN14_S

PE_A_RXP15_S

PE_A_RXN15_S

PE_A_RXP16_S

PE_A_RXN16_S

PE_A_RXP17_S

PE_A_RXN17_S

PE_A_RXP18_S

PE_A_RXN18_S

PE_A_RXP19_S

PE_A_RXN19_S

PE_A_RXP20_S

PE_A_RXN20_S

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

PE_A_RXP13_S

PE_A_RXN13_S

PE_A_RXP14_S

PE_A_RXN14_S

PE_A_RXP15_S

PE_A_RXN15_S

PE_A_RXP16_S

PE_A_RXN16_S

PE_A_RXP17_S

PE_A_RXN17_S

PE_A_RXP18_S

PE_A_RXN18_S

PE_A_RXP19_S

PE_A_RXN19_S

PE_A_RXP20_S

PE_A_RXN20_S

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

PE_A_RXP13_S

PE_A_RXN13_S

PE_A_RXP14_S

PE_A_RXN14_S

PE_A_RXP15_S

PE_A_RXN15_S

PE_A_RXP16_S

PE_A_RXN16_S

PE_A_RXP17_S

PE_A_RXN17_S

PE_A_RXP18_S

PE_A_RXN18_S

PE_A_RXP19_S

PE_A_RXN19_S

PE_A_RXP20_S

PE_A_RXN20_S

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

PE_A_RXP13_S

PE_A_RXN13_S

PE_A_RXP14_S

PE_A_RXN14_S

PE_A_RXP15_S

PE_A_RXN15_S

PE_A_RXP16_S

PE_A_RXN16_S

PE_A_RXP17_S

PE_A_RXN17_S

PE_A_RXP18_S

PE_A_RXN18_S

PE_A_RXP19_S

PE_A_RXN19_S

PE_A_RXP20_S

PE_A_RXN20_S

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

PE_A_RXP13_S

PE_A_RXN13_S

PE_A_RXP14_S

PE_A_RXN14_S

PE_A_RXP15_S

PE_A_RXN15_S

PE_A_RXP16_S

PE_A_RXN16_S

PE_A_RXP17_S

PE_A_RXN17_S

PE_A_RXP18_S

PE_A_RXN18_S

PE_A_RXP19_S

PE_A_RXN19_S

PE_A_RXP20_S

PE_A_RXN20_S

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

PE_A_RXP13_S

PE_A_RXN13_S

PE_A_RXP14_S

PE_A_RXN14_S

PE_A_RXP15_S

PE_A_RXN15_S

PE_A_RXP16_S

PE_A_RXN16_S

PE_A_RXP17_S

PE_A_RXN17_S

PE_A_RXP18_S

PE_A_RXN18_S

PE_A_RXP19_S

PE_A_RXN19_S

PE_A_RXP20_S

PE_A_RXN20_S

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

PE_A_RXP13_S

PE_A_RXN13_S

PE_A_RXP14_S

PE_A_RXN14_S

PE_A_RXP15_S

PE_A_RXN15_S

PE_A_RXP16_S

PE_A_RXN16_S

PE_A_RXP17_S

PE_A_RXN17_S

PE_A_RXP18_S

PE_A_RXN18_S

PE_A_RXP19_S

PE_A_RXN19_S

PE_A_RXP20_S

PE_A_RXN20_S

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

PE_A_RXP13_S

PE_A_RXN13_S

PE_A_RXP14_S

PE_A_RXN14_S

PE_A_RXP15_S

PE_A_RXN15_S

PE_A_RXP16_S

PE_A_RXN16_S

PE_A_RXP17_S

PE_A_RXN17_S

PE_A_RXP18_S

PE_A_RXN18_S

PE_A_RXP19_S

PE_A_RXN19_S

PE_A_RXP20_S

PE_A_RXN20_S

+12V

VCC3

PLTRST_BU2# 18,20,21

CK_8PORT_DP

PE_A_RXP8_S

PE_A_RXN8_S

PE_A_RXP9_S

PE_A_RXN9_S

PE_A_RXP10_S

PE_A_RXN10_S

PE_A_RXP11_S

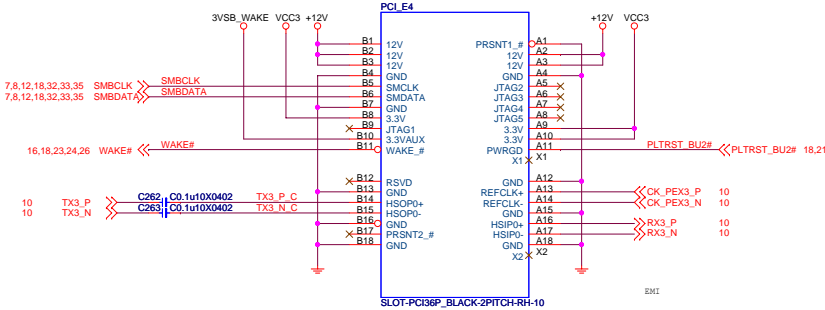
PE_A_RXN11_S

PE_A_RXP12_S

PE_A_RXN12_S

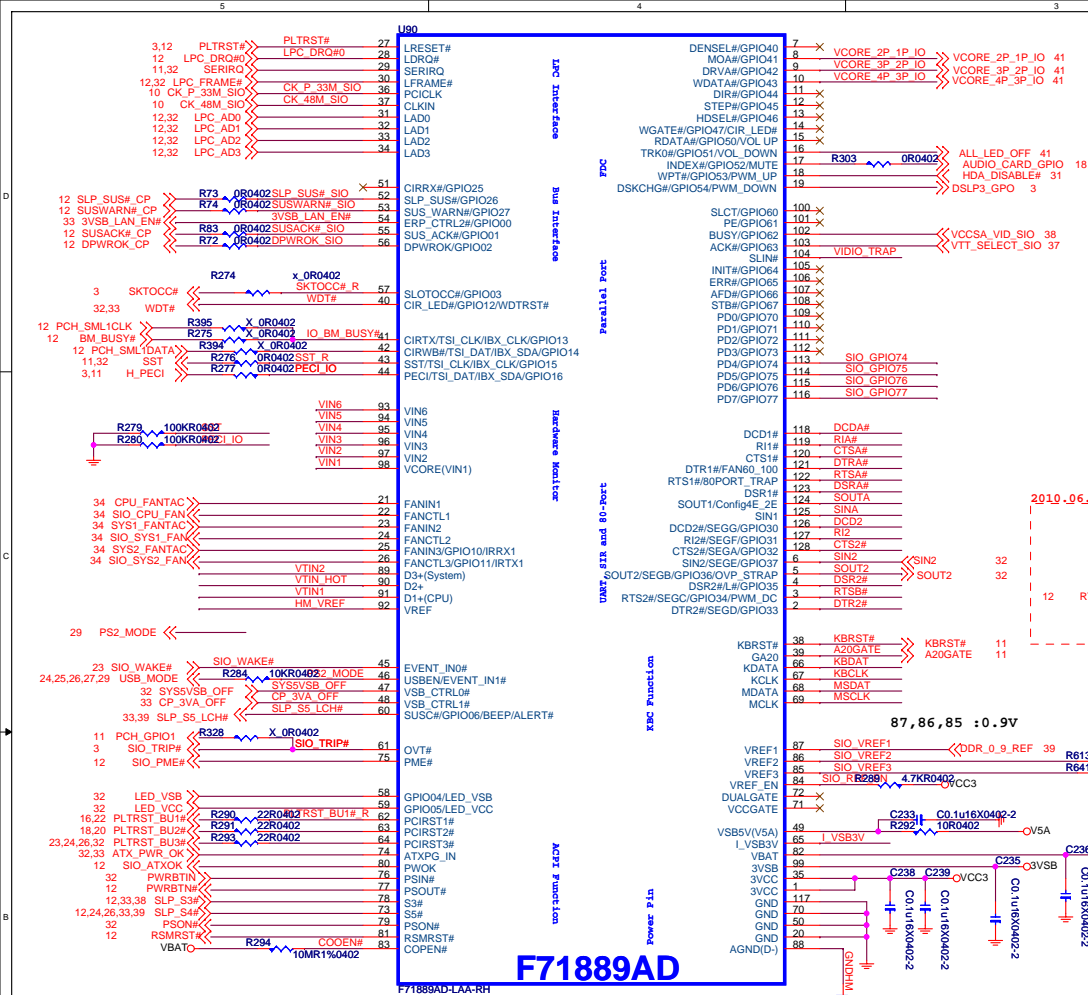
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PCI EXPRESS x1-PORT



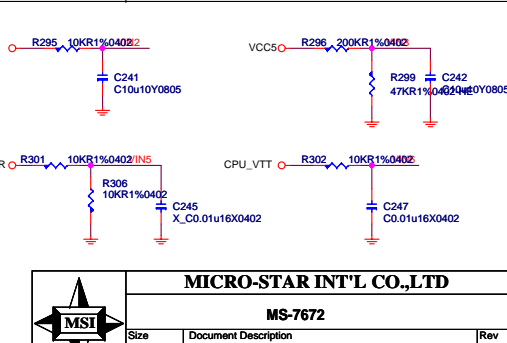
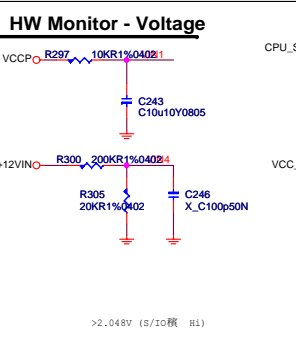
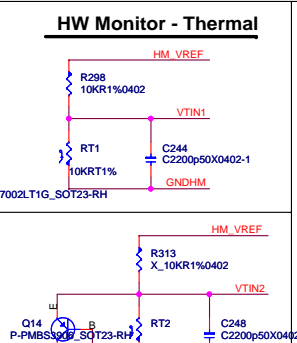
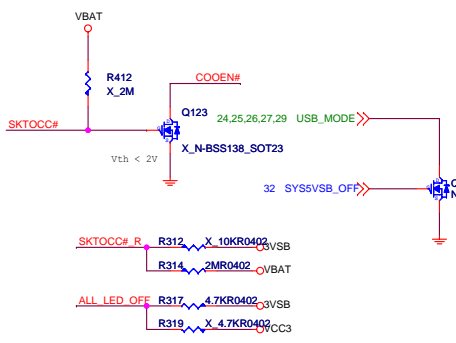
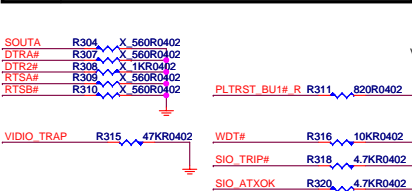
PCI EXPRESS x1-PORT

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Size	Custom	Document Number	Rev	
Date:	Tuesday, November 30, 2010	Sheet	20	of 40

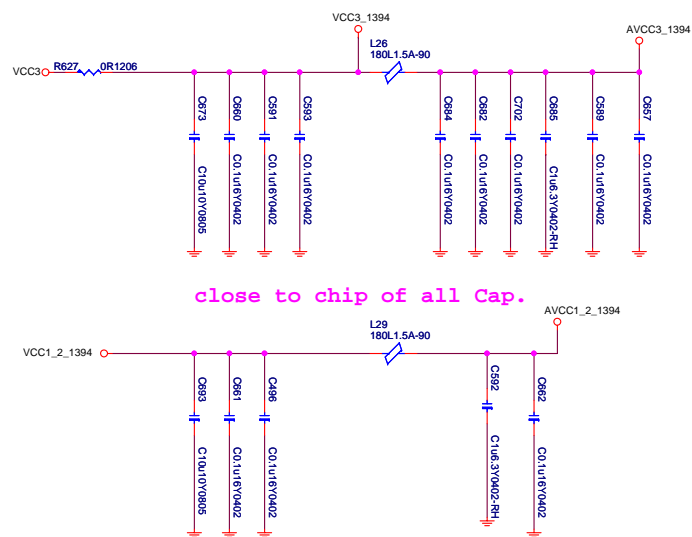
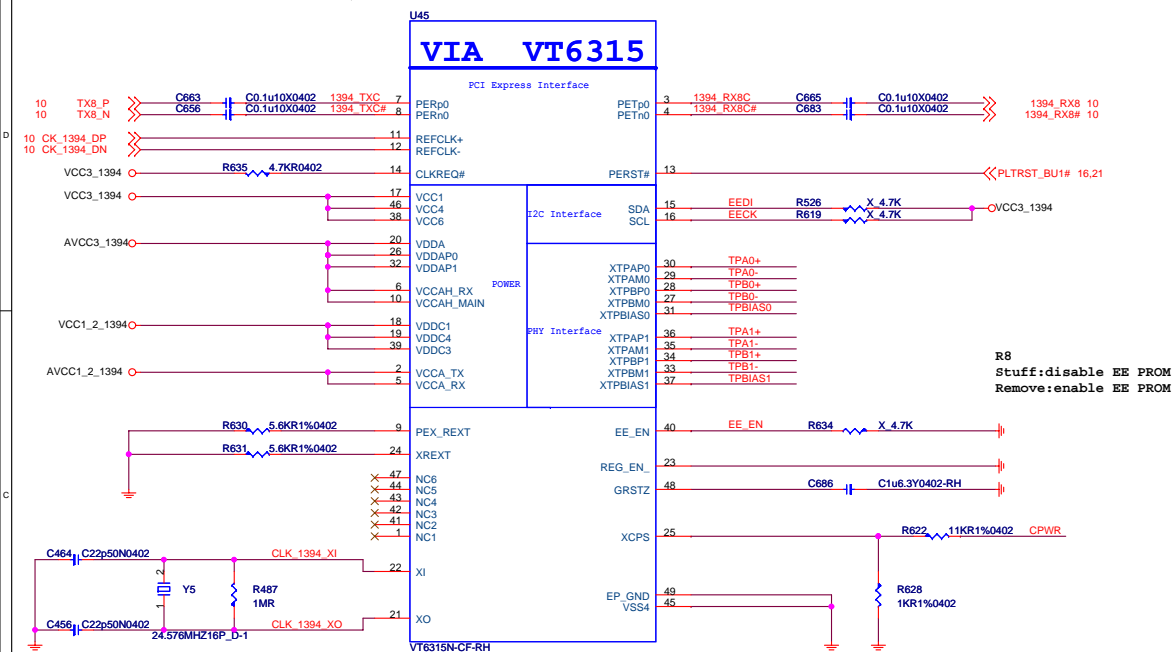


LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

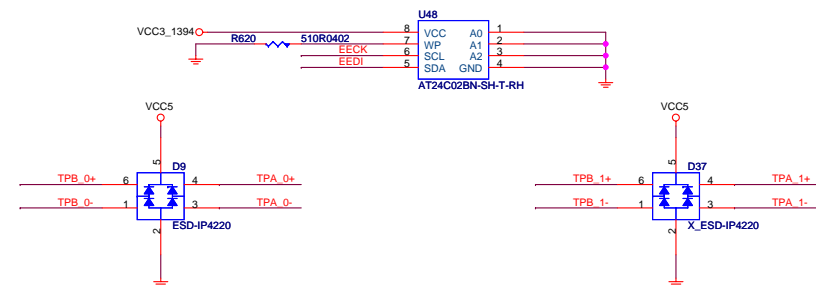
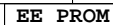
STRAP	Don't STUFF	STUFF
SOUTA#	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
DTR2#	PIN51-56=GPIO	PIN51-56=BUS
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80Port ENABLE	80 Port DISABLE
SLIN#	PD 47K, pin 100-103 and pin105-116 as GPIO pin	



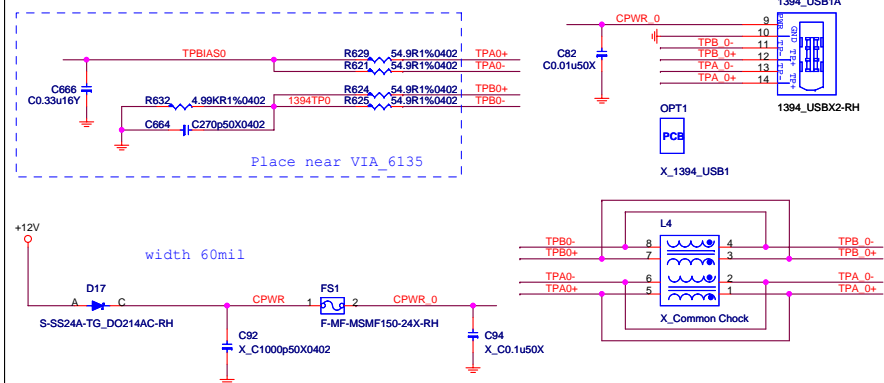
1394 CONTROLLER



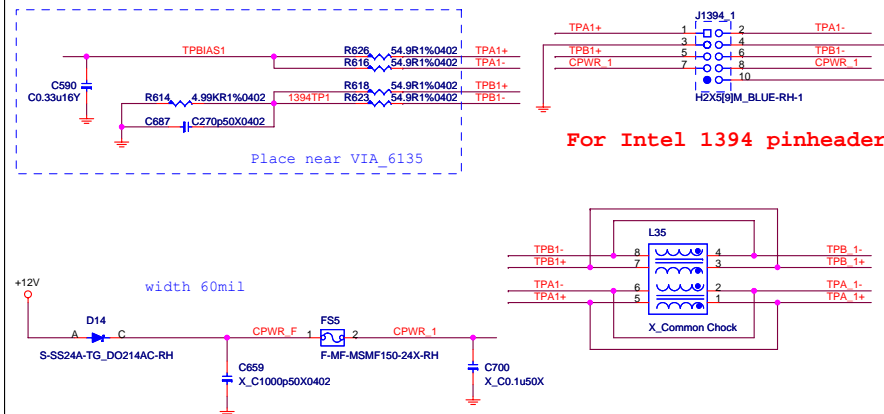
close to chip of all Cap.



Rear 1394 port



Front 1394 pin header



MICRO-STAR INT'L CO.,LTD

MS-7678

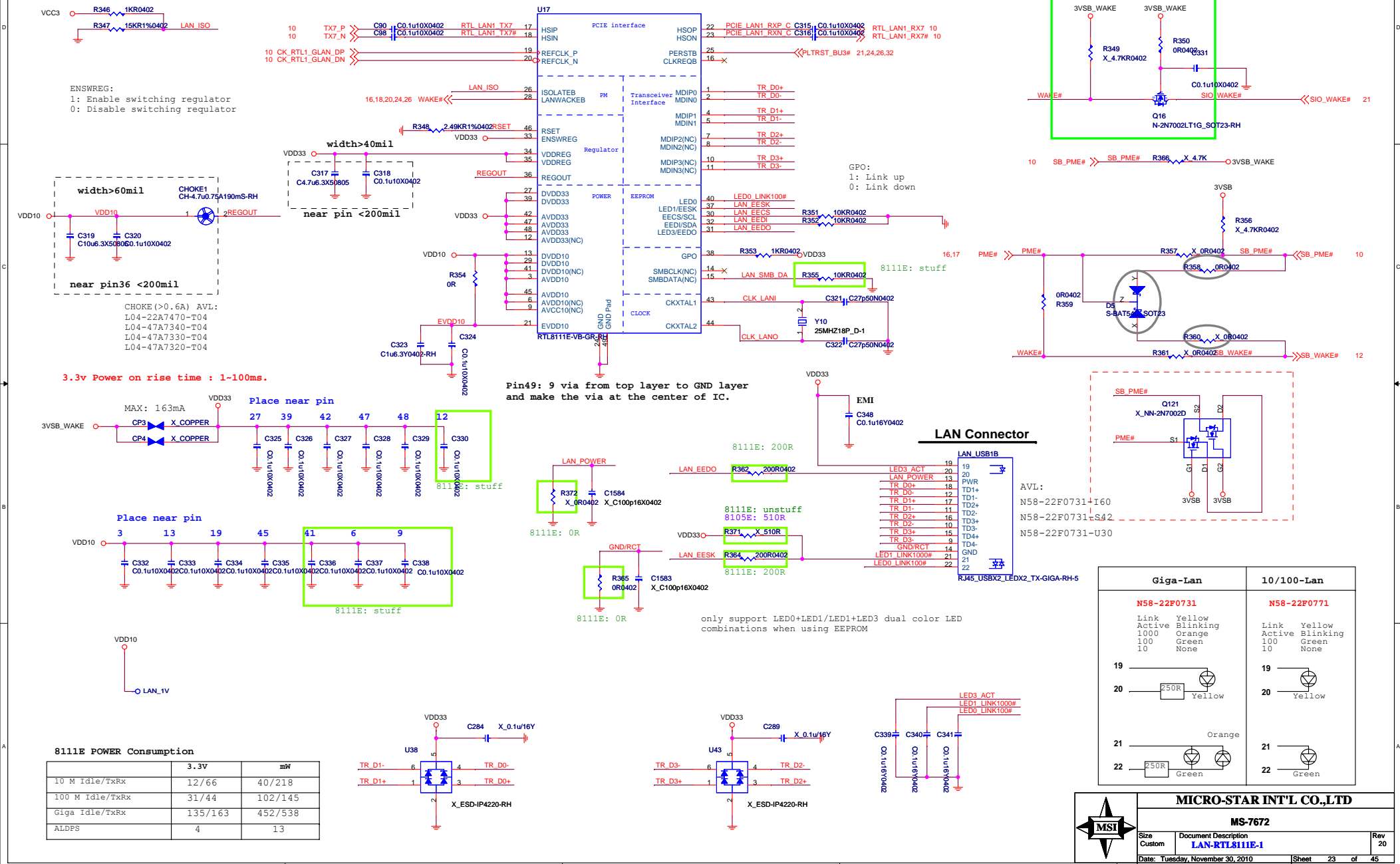
Size Custom	Document Description 1394 Controller - VT6315N-CE
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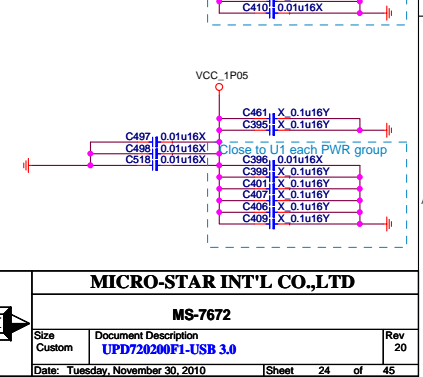
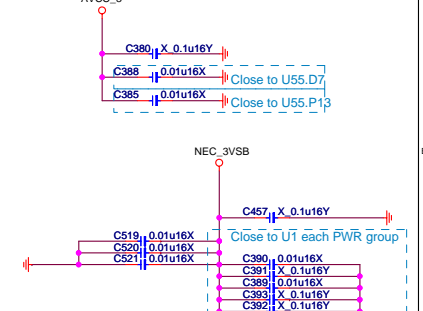
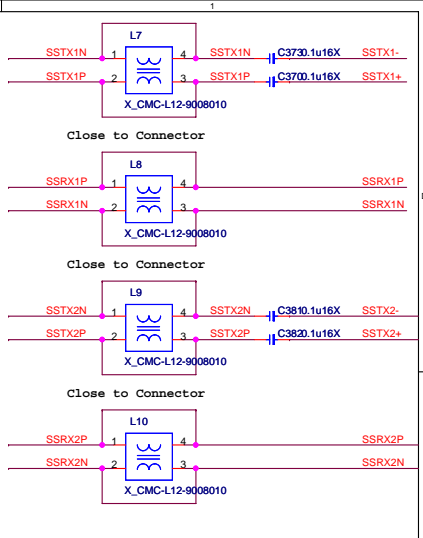
Rev	20
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Date: Tuesday, November 30, 2010 Sheet 22 of 46

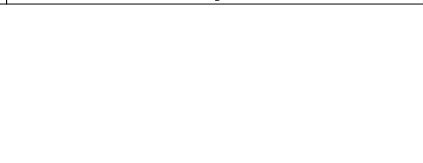
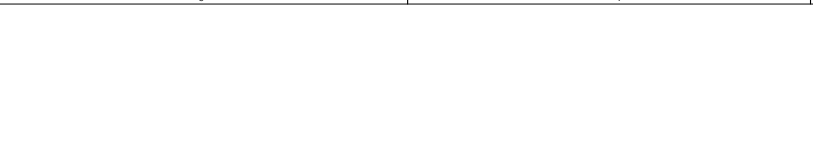
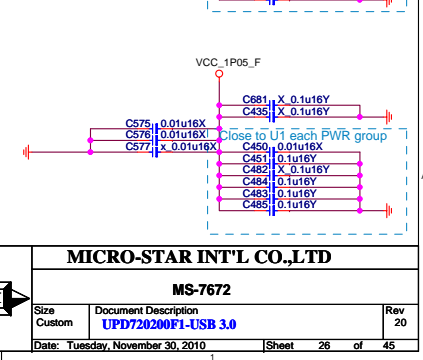
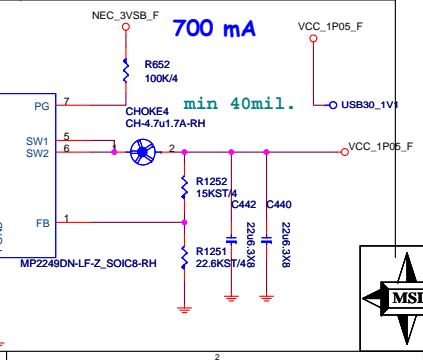
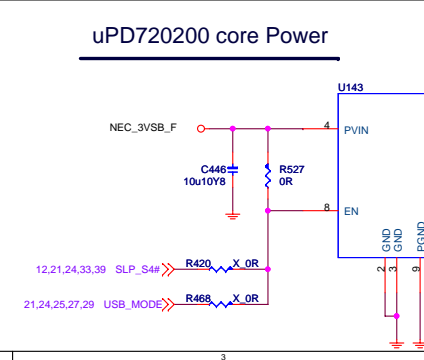
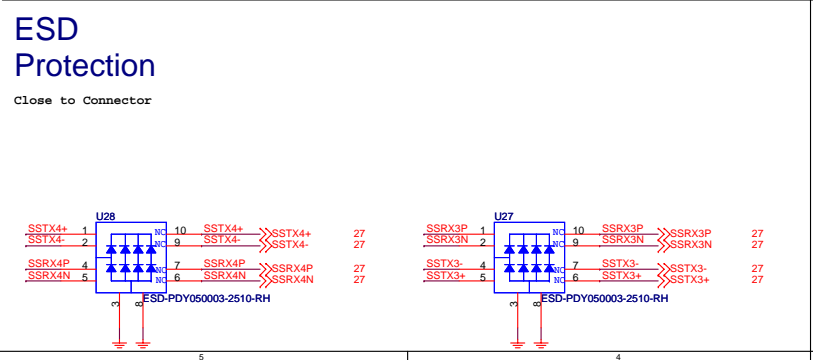
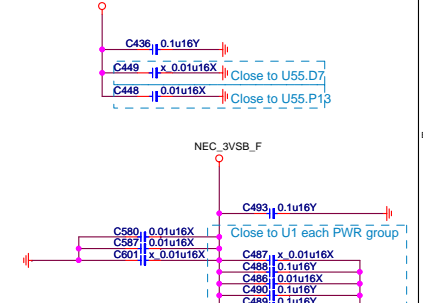
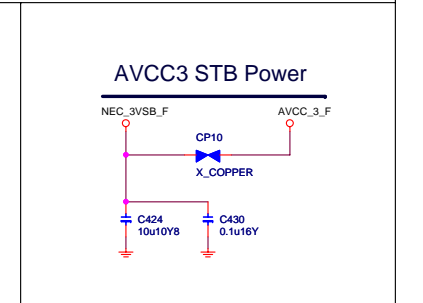
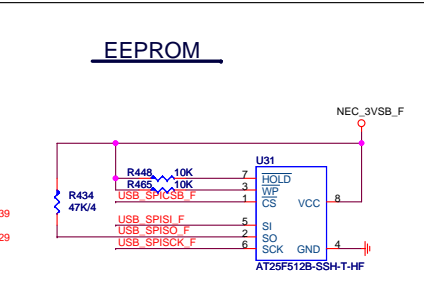
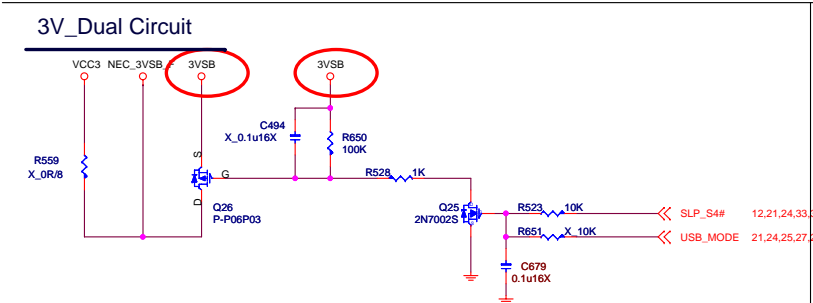
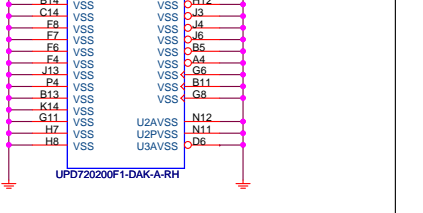
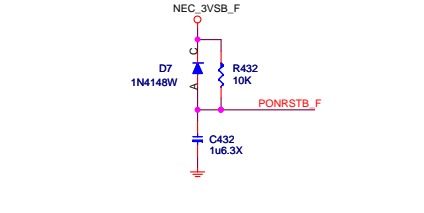
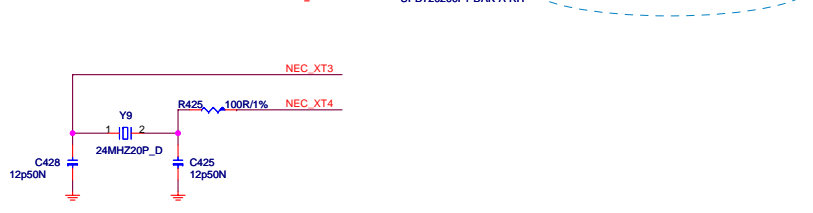
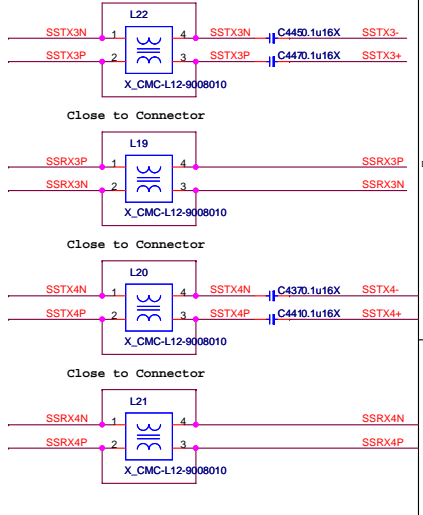
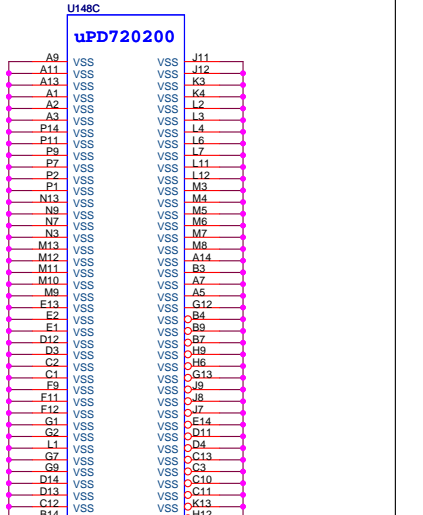
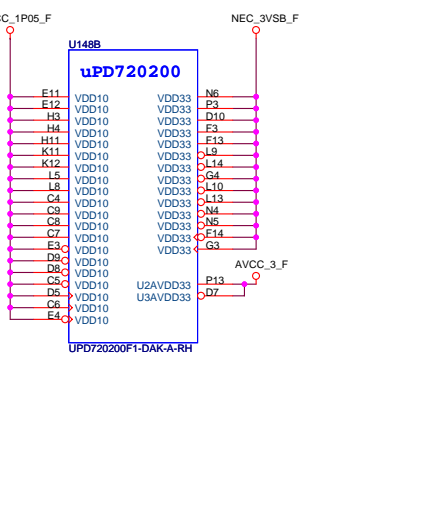
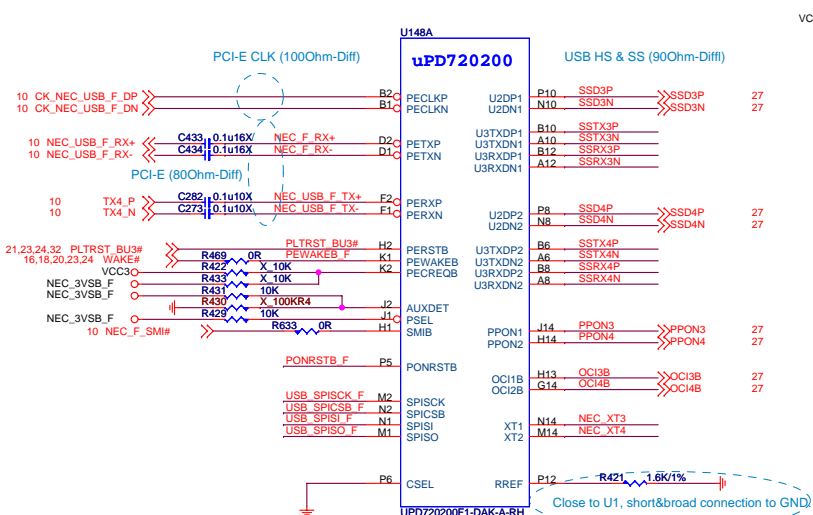
RTL8111E Giga LAN

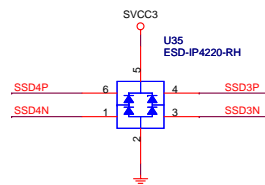
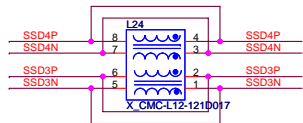
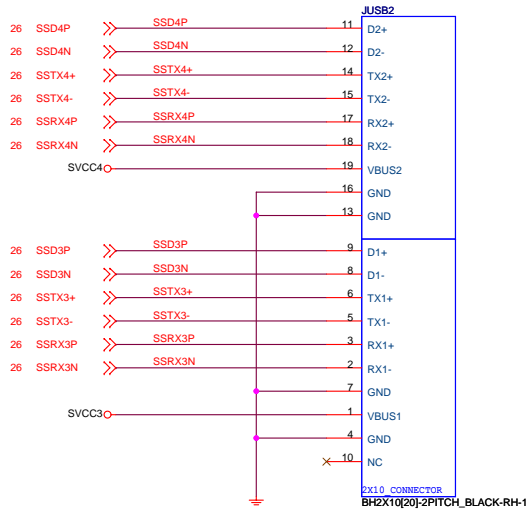
LAN/PCIE/PCI Wake Up CTRL Circuit



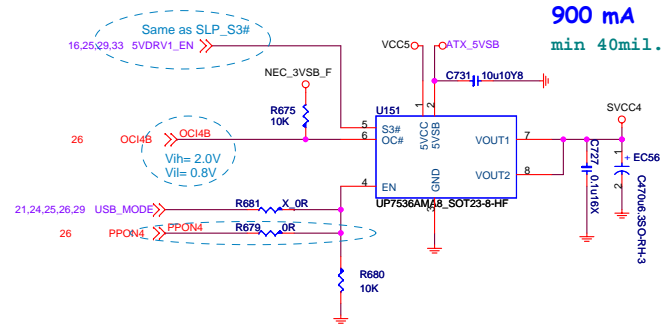
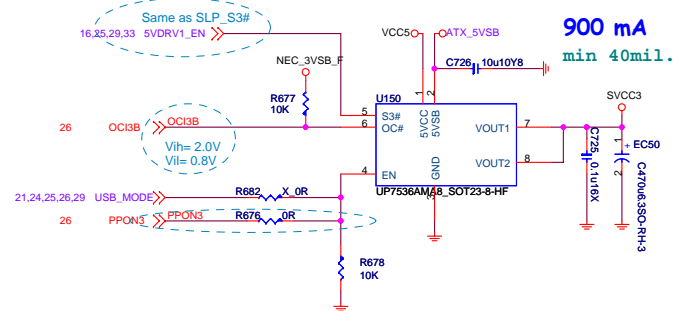








All power sources of uPD720200 are supplied, PPNx is enable.
 PPNx is low when OCix going to low.



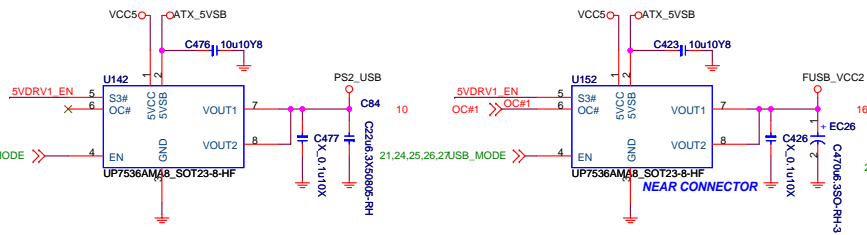
MICRO-STAR INT'L CO.,LTD

MS-7672

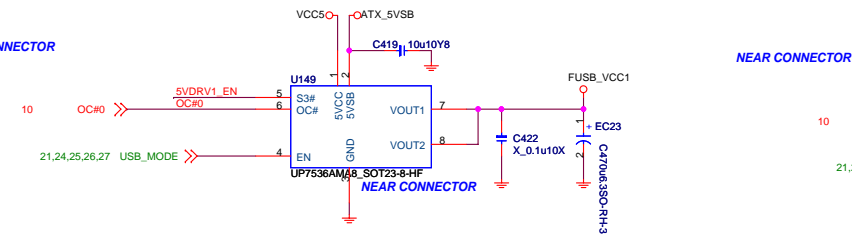
Size Custom	Document Description USB 3.0 Power & Connector	Rev 20
Date: Tuesday, November 30, 2010	Sheet 27 of 45	

Front USB Connector

USB POWER FOR PORT 11,12

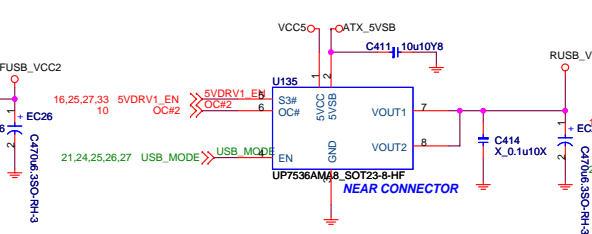


USB POWER FOR PORT 11,12

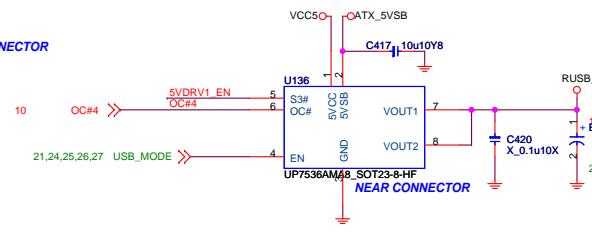


Rear USB Connector

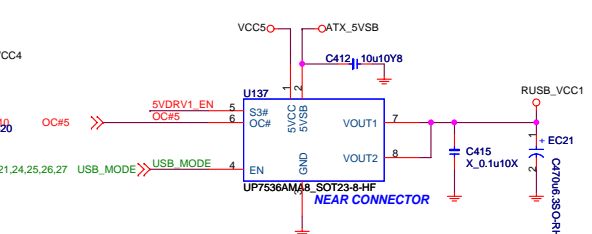
USB POWER FOR PORT 4,5



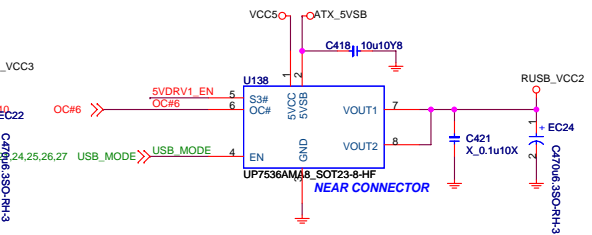
USB POWER FOR PORT 11,12



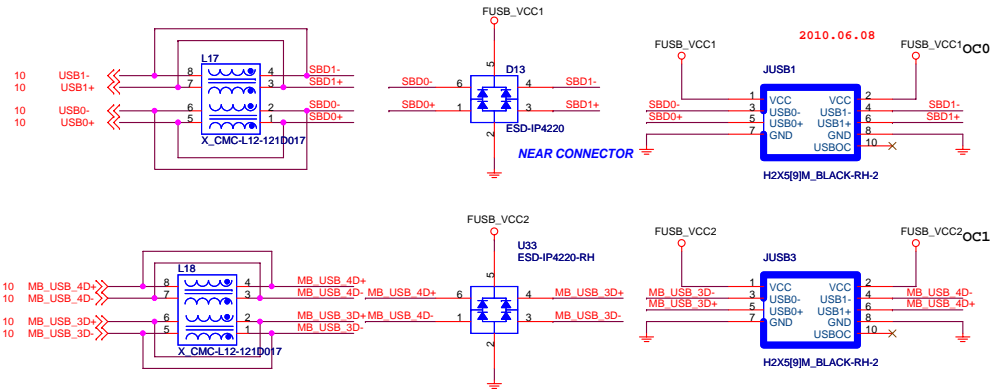
USB POWER FOR PORT 6,7



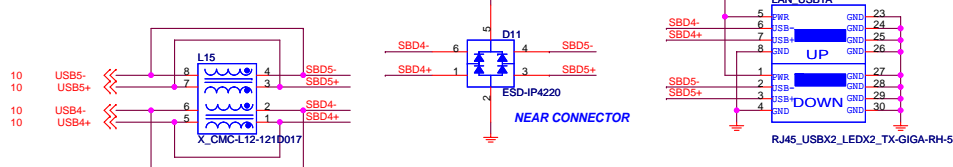
USB POWER FOR PORT 8,9



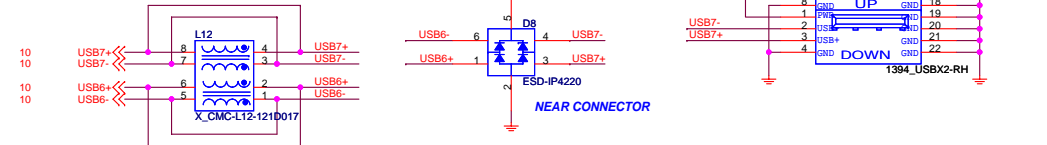
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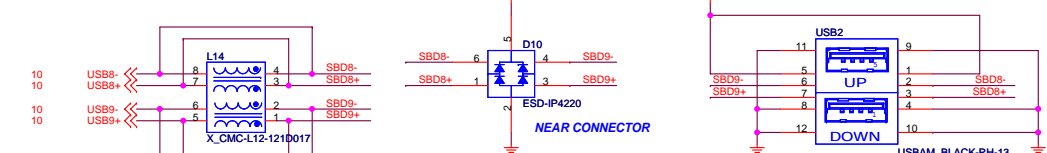
FRONT USB PORT 4,5(With RJ45)



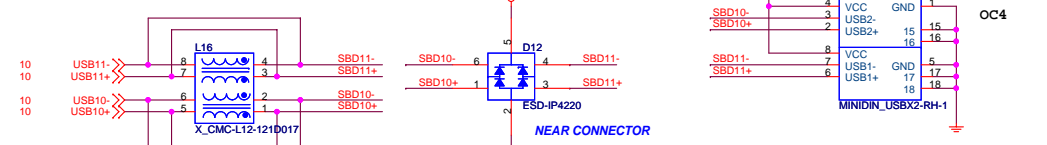
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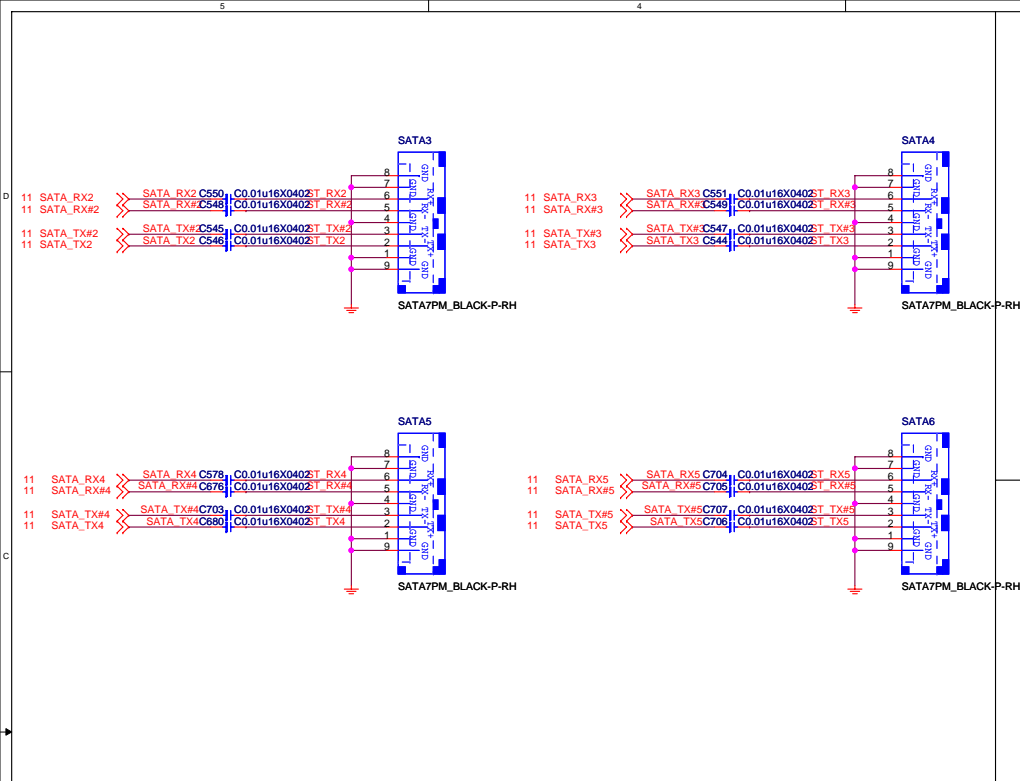
REAR USB PORT 8,9 (With ESATA)



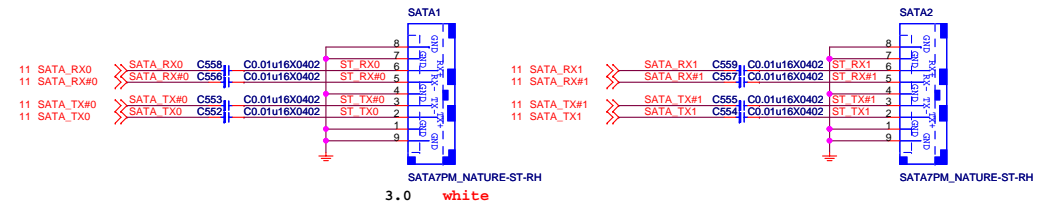
REAR USB PORT 8,9 (With PS2)



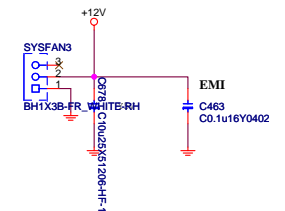
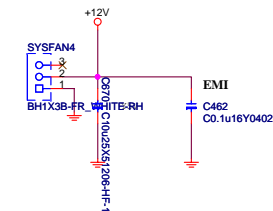
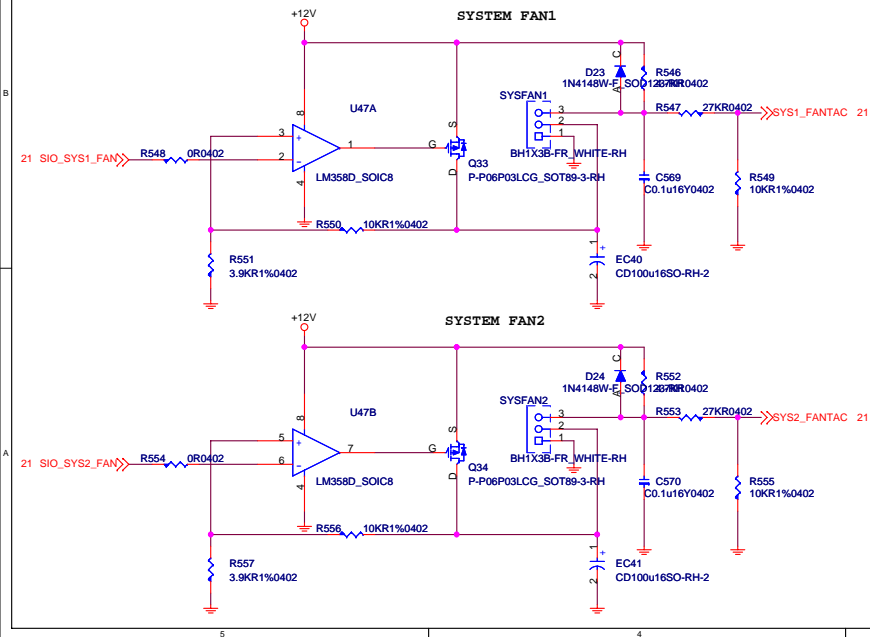
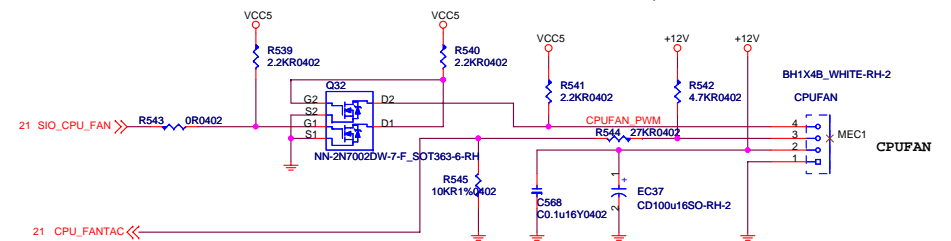
MICRO-STAR INT'L CO.,LTD		
MS-7672		
Size	Document Description	Rev
Custom	USB Connectors-12port	20
Date: Tuesday, November 30, 2010	Sheet 29	of 45



SATA 6G PORT 0,1



CPU FAN-CONTROL CIRCUIT

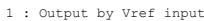


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MS-7672

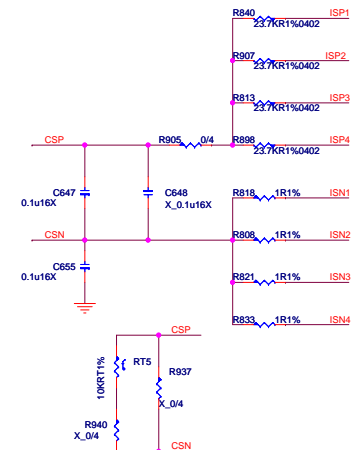
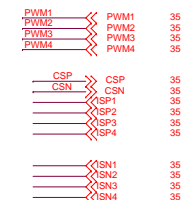
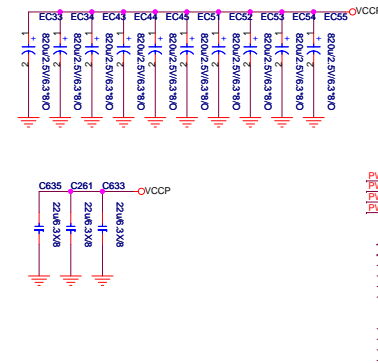
Size	Document Description	Rev
Custom	SATA & e-SATA Ports and Fan Control	20
Date:	Tuesday, November 30, 2010	Sheet 34 of 45

CPU VTT 3VSB



MS-7672

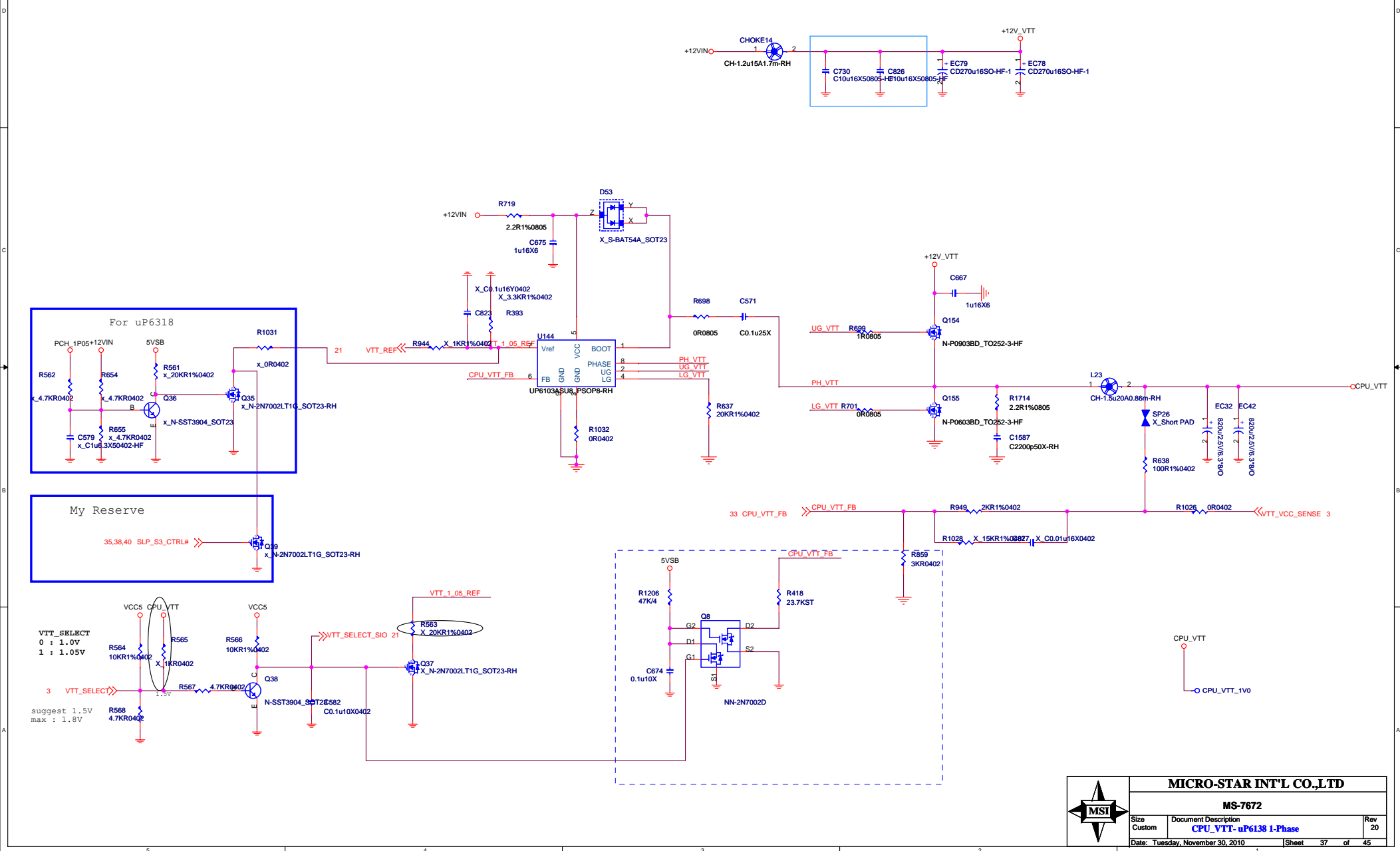
Size Custom	Document Description VRD12 - ISL6234 6+2Phase	Rev 20
Date: Tuesday, November 30, 2010		Sheet 35 of 45



CPU VTT 8.2A

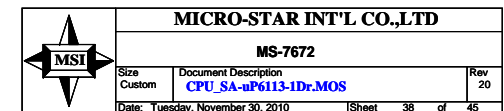
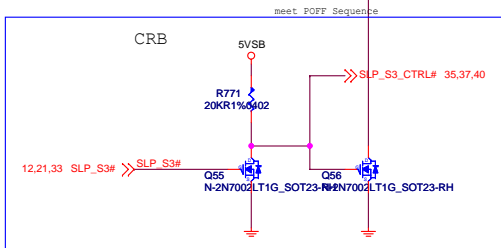
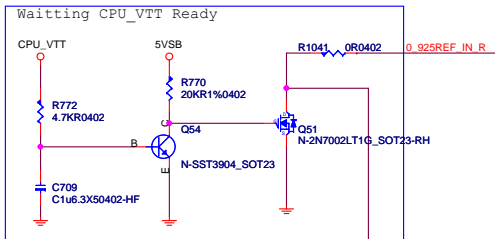
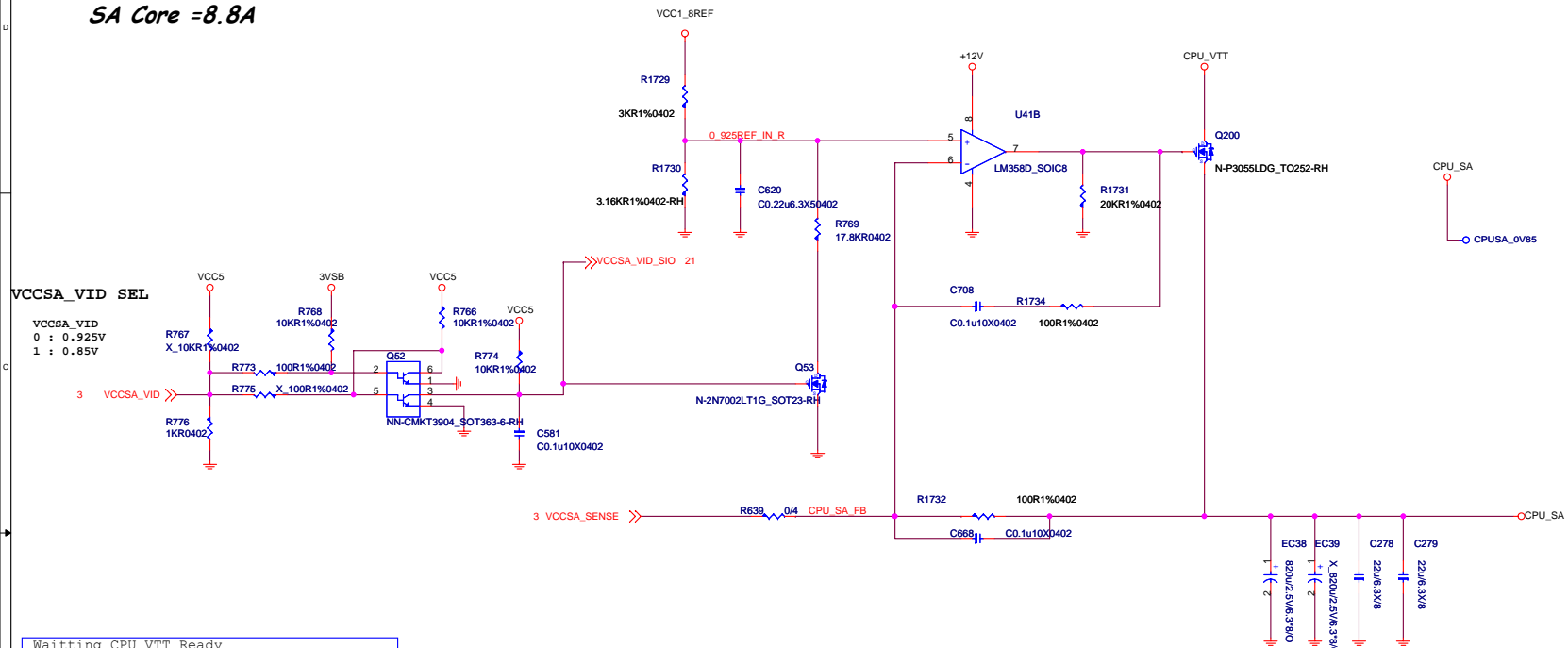
$$I_{ripple} = 1.9(v_{tt}) + 1.8(s_a)$$

$$5 \times 2 = 10A > 3.8A$$



SA Core = 8.8A

8.8A



4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT



DDR VTT Power

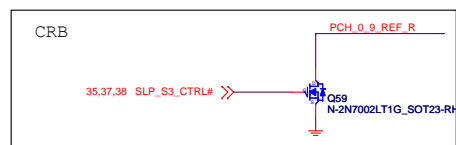
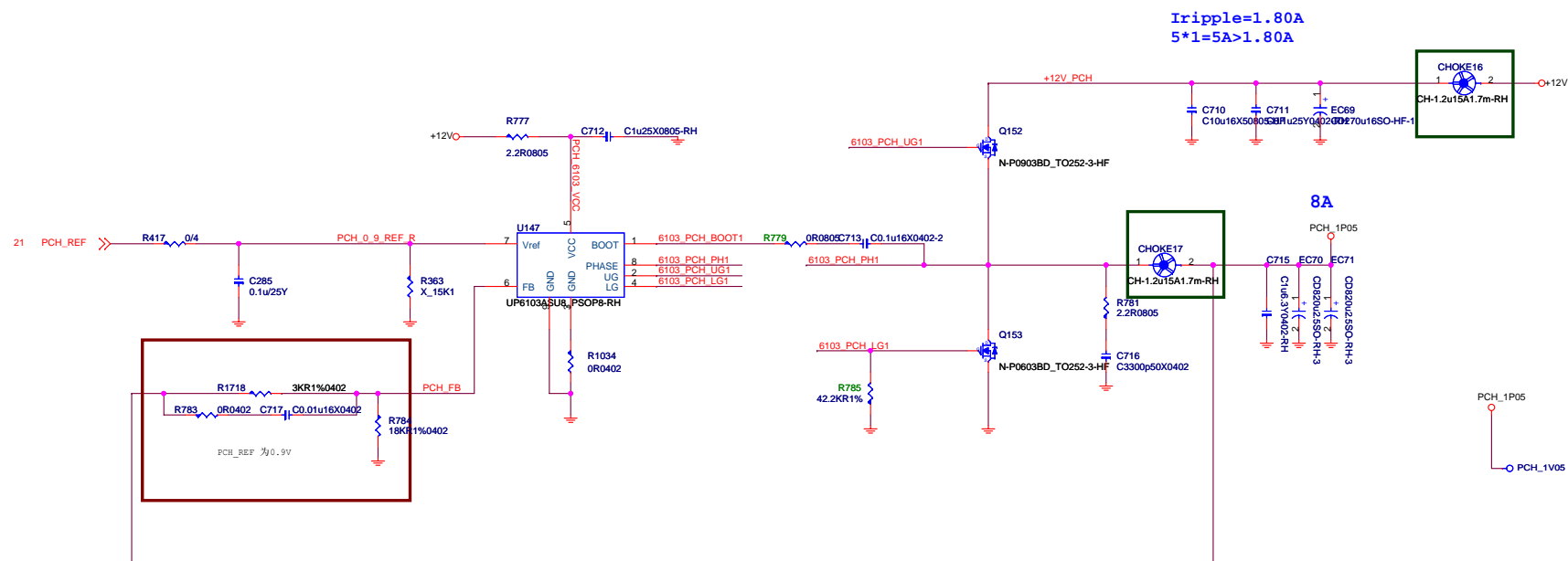
[illegible]

MS-7672

Rev	20
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Date: Tuesday, November 30, 2010 Sheet 39 of 45

PCH Core $6.2A + 1.8A = 8A$



	uP6103A	uP6138
PIN1	BOOT	BOOT
PIN2	UG	UG
PIN3	GND	VREFIN
PIN4	LG	LG
PIN5	VCC	VCC
PIN6	FB	FB
PIN7	Vref	OCP/EN
PIN8	PHASE	PHASE
PIN9	GND	GND



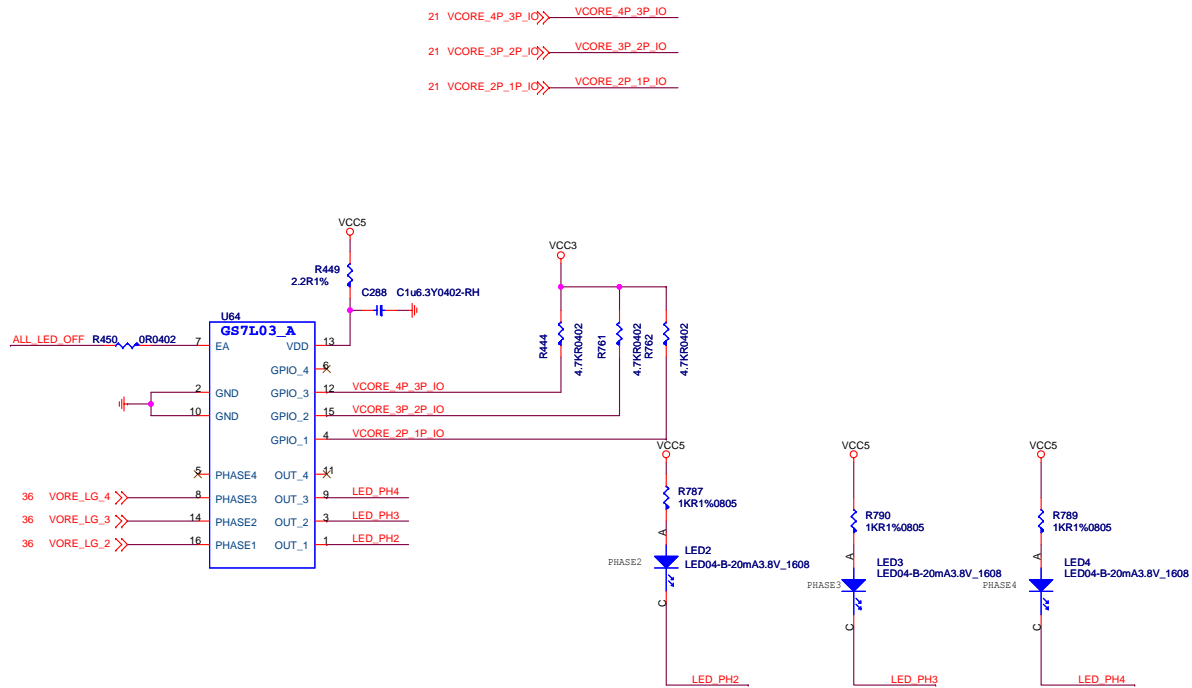
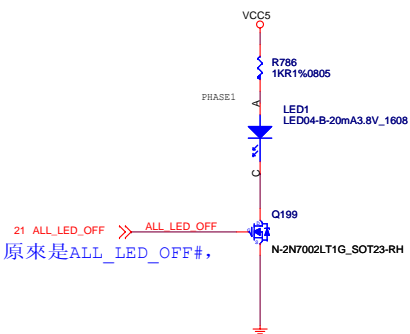
MICRO-STAR INT'L CO.,LTD

MS-7672

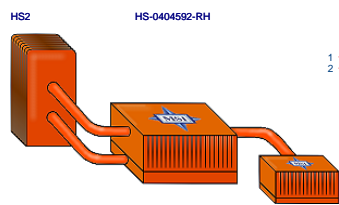
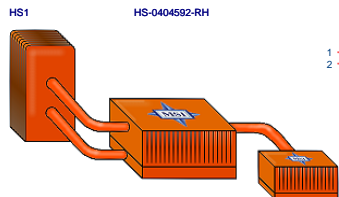
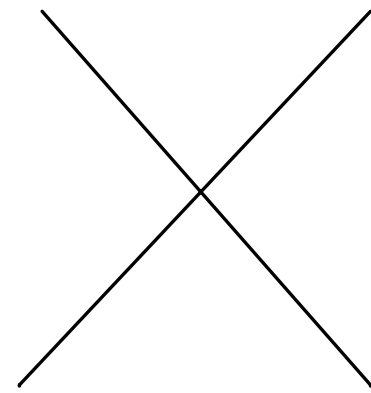
Size Custom	Document Description PCH Power - uP6103 1-Phase
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Date: Tuesday, November 30, 2010	Sheet 40 of 45
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all on board LED switch



MICRO-STAR INT'L CO.,LTD		
MS-7672		
Size Custom	Document Description PHASE Dropping & LED	Rev 20
Date: Tuesday, November 30, 2010		Sheet 41 of 45



1

2

1

2



Rubber



Rubber



THX



label



BAT-BCR2032P-RH



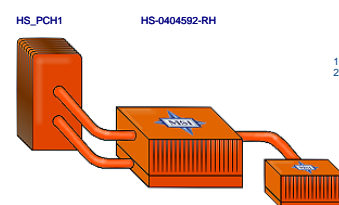
E21-7557040-L06



7581_11

PD0-0758111-E48, 腦地, 27, 腳
PD0-0758111-G37, 弘0, 27, 腳

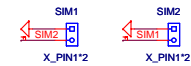
吹邻紅 (MSIS)
吹邻紅 (MSIS)



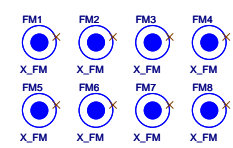
1

2

Simulation

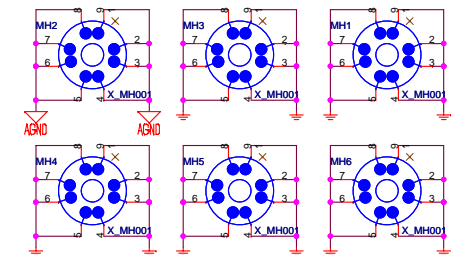


Optical Fiducial Marks-120



Optical Fiducial Marks-100

Mounting Holes



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MS-7672

Size	Custom	Document Description	XDP / Manual Parts	Rev	20
Date:	Tuesday, November 30, 2010	Sheet	42 of 45		